

DesignCon 2020

Current Distribution, Resistance, and Inductance in Power Connectors

Adam Gregory, Samtec
adam.gregory@samtec.com

Clement Luk, Samtec
clement.luk@samtec.com

Gary Biddle, Samtec
gary.biddle@samtec.com

Gustavo Blando, Samtec
gustavo.blando@samtec.com

Istvan Novak, Samtec
istvan.novak@samtec.com

Abstract

This paper analyzes the frequency dependent resistance and inductance of power connector pin patterns. The details of a single power pin are analyzed, and the final results come from parametric studies of pin arrays that are part of specific printed circuit board layouts. The results of this study have 2 significant outcomes to the designer utilizing a power connector. 1) A layout that minimizes individual power pin current will minimize system power consumption. 2) An accurate representation of frequency dependent resistance and inductance can be used to strategically optimize signal-to-power pin isolation to reduce noise.

Author(s) Biography

Adam Gregory is a Signal Integrity Engineer at Samtec. He is involved in modeling and analysis of high-speed differential signaling channels. He received a BSEE and MSEE at the University of South Carolina.

Clement Luk is a Signal Integrity Engineer in Samtec. He is involved in high-speed connector, PCIe application and channel simulation and measurement. He received his BSCS and MSEE from University of Wisconsin-Madison.

Gustavo Blando is a Senior Principal Engineer and leading Principal SI/PI Architect at Samtec Inc. In addition to his leadership roles, he's charged with the development of new SI/PI methodologies, high speed characterization, tools and modeling in general. Gustavo has twenty plus years of experience in Signal Integrity and high-speed circuits.

Gary Biddle received his BS in Physics from University of Florida 1976 and MS in Physics from Penn State University 1991. His work experience includes high frequency VNA and EMI measurements, along with nearly 20 years of simulating PCB and interconnect structures. He has published several articles and holds several patents.

Istvan Novak is a Principal Signal and Power Integrity Engineer at Samtec, working on advanced signal and power integrity designs. Prior to 2018 he was a Distinguished Engineer at SUN Microsystems, later Oracle. He worked on new technology development, advanced power distribution and signal integrity design and validation methodologies for SUN's successful workgroup server families. He introduced the industry's first 25um power-ground laminates for large rigid computer boards and worked with component vendors to create a series of low-inductance and controlled-ESR bypass capacitors. He also served as SUN's representative on the Copper Cable and Connector Workgroup of InfiniBand, and was engaged in the methodologies, designs and characterization of power-distribution networks from silicon to DC-DC converters. He is a Life Fellow of the IEEE with twenty-five patents to his name, author of two books on power integrity, teaches signal and power integrity courses, and maintains a popular SI/PI website.

I. Introduction

This paper analyzes the frequency dependent resistance and inductance of various power connector pin patterns and connection geometries. Initially the details of a single power pin is analyzed, and the final results come from parametric studies of pin arrays that are part of specific printed circuit board layouts. With the availability of detailed DC solvers using fine mesh, the DC and low-frequency current distribution in power structures has previously been analyzed [1] for printed circuit boards that contain layer transitions with a multitude of vias.

It was shown that for the same number of connecting vias, the current per via strongly depends on the via pattern. When power connectors are used between two printed circuit boards, the connector pins in an array work similarly to vias in a via array. This suggests that the total current per pin and the current distribution inside each pin can be a function of the geometry in the connecting boards [2]. As a result, the actual performance of the power connector can't be fully analyzed without knowing the surrounding printed circuit board geometry selected by the user. The results of this study have two significant outcomes to the designer utilizing a power connector. 1) A layout that optimizes current distribution across connector pins and thus improves power delivery. 2) An accurate representation of frequency dependent resistance and inductance in the relevant spectrum can be used to strategically optimize primarily the signal-to-power pin isolation to reduce noise coupling between signal pins and pins used to carry power and the potential coupling of noise between different power pins.

The simulation results start by analyzing an isolated power pin and pin pair case. The analysis follows with a power connector placed in between two printed circuit boards. The printed circuit board layout is selected to match an existing power connector design, so simulation to measurement correlation can be performed.

The results from the study answer the following questions. How does material and power pin geometry impact frequency dependent resistance and inductance? How do material properties change current distributions in complex geometries and layered metals? How does the layout of the printed circuit board that is attached to the connector impact the current distribution, resistance, and inductance inside the power pins and on the PCB planes? What general connector pin geometries and pin assignments are better for printed circuit board layouts?

In addition, we explore utilizations of open pin-field connectors to supply power. A board designer often needs to allocate signal pins to carry current. How will the placement of power pins affect neighboring signal pins? What is the impact of connector location and pin assignment on power-to-signal crosstalk? We explore the spatial aspect of a power distribution system with connectors and its impact to signal integrity.

We look at three different connector families: a blade type connector, primarily designed to carry high currents instead of high-speed signals, a pin-array type connector that can be configured to carry high-speed signals or medium power-rail currents, and a mixed type connector, which has an open pin field array and power blades in the same shroud.

II. Single Power Path

We first look at a single interconnect to understand the frequency dependence of its parameters. For high-speed connectors, full-wave models are typically provided as S parameters in Touchstone format. These models, however, often start at 10MHz and may not even have a DC data point. By doing so we potentially lose the frequency dependent variations that happens due to the early development of skin effect at lower frequencies.

To cover the important frequency range necessary for power applications, we start our data sets at 1kHz or lower and obtain a DC point separately. At low frequencies the resistance and inductance of the series path is dominant and we can largely ignore the capacitance and conductance of the parallel path.

Coaxial Cable

As a starting point, we look at a coaxial cable with its resistance and inductance. Figure II-1 shows a coaxial cable with copper conductors and homogeneous dielectric material and its frequency-dependent resistance and inductance. The analytical values for resistance and inductance are plotted alongside the simulated results. The analytical inductance assumes that the imaginary part of resistance is identical to the real part of resistance, but this breaks down when the skin depth is larger than the conductor radius. We use these results as a calibration point for our simulator settings.

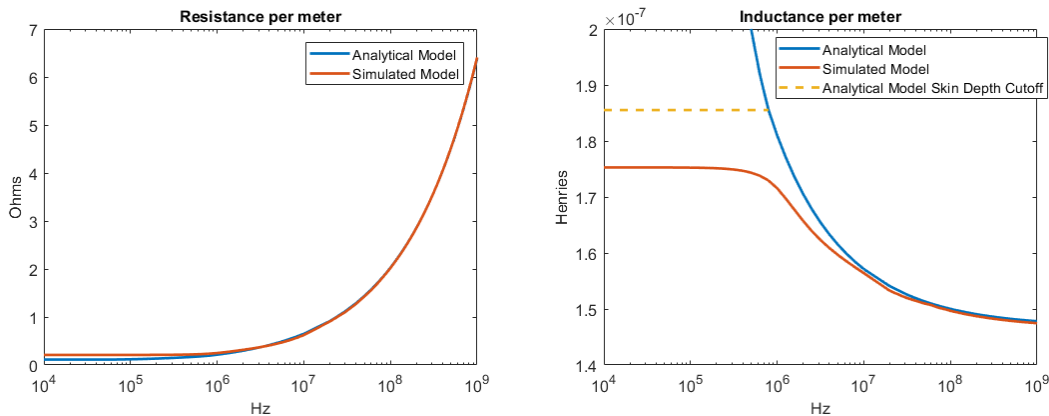


Figure II-1: Resistance and Inductance of coaxial cable

The coaxial cable signal conductor radius (r_1) was 12 mils. The dielectric radius (r_2) was 25 mils. The signal and ground conductor used copper with conductivity set to $5.8e7$ S/m. The equations below show the analytical calculations used to predict resistance and inductance per meter.

$$\delta = \sqrt{\frac{2}{\omega\sigma\mu}} \quad (\text{Equation 1})$$

The skin depth (δ) is used to calculate resistance per meter in Equation 2.

$$\text{Resistance per meter} = R = \frac{1}{\sigma(2\pi r_1 \delta - \pi \delta^2)} + \frac{1}{\sigma(2\pi r_2 \delta + \pi \delta^2)} \quad (\text{Equation 2})$$

$$\text{Inductance per meter} = \frac{\mu}{2\pi} \log \frac{r_2}{r_1} + \frac{R}{\omega} \quad (\text{Equation 3})$$

Pin Loop with Layered Metal

After verifying coaxial cable results, we move to a simple example that approximates a connector: a cylindrical power and ground pin inside a homogeneous dielectric material. When using a limited-size geometry, detailed inside layered conductors may be possible to simulate. Once we draw our conclusions, for multi-pin connector arrays we can simplify the analysis by replacing the layered conductors with an equivalent single material.

Interconnect material is seldom pure copper for various reasons. For both cable wires and connector pins, the core tends to be steel alloy, brass or phosphor bronze. These materials are used to provide mechanical strength, flexibility, but are much poorer electrical conductors. At high frequencies this is compensated by plating with a thin layer of better conductor: copper or gold. Gold plating requires an underlying Nickel boundary, which is also relatively poor conductor, and it is ferromagnetic. This will result in a stronger frequency dependent resistance and inductance.

Figure II-2 shows frequency dependent resistance and inductance as a comparison between single conductive material and layered conductive material for 2 pins placed in homogeneous dielectric material. For each case, the full radius of each pin is 10 mils and the center to center pitch between pins is 40 mils. (This is 20 mils edge to edge separation). The copper pins have conductivity set to $5.8e7$ S/m. The layered pins have a 9 mil radius Beryllium core with a 1 mil layer of copper on the outside. The conductivity of Beryllium is set to $2.5e7$ S/m. The dielectric material surrounding the pins has a dielectric constant of 4.4.

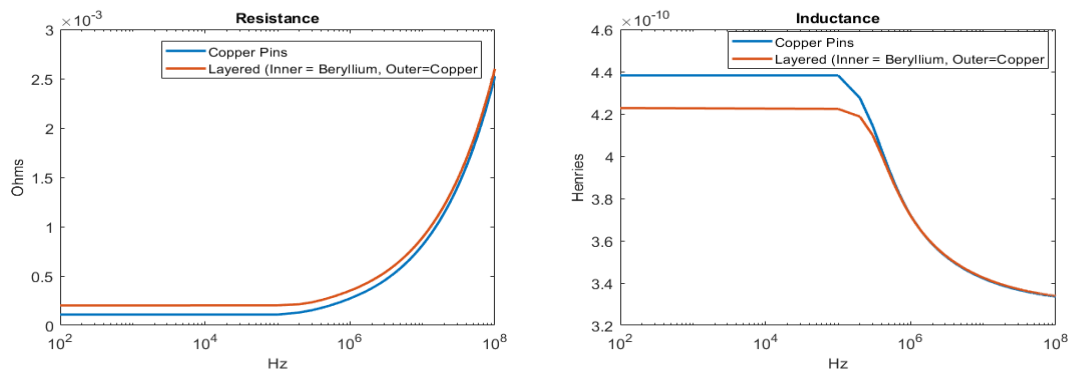


Figure II-2: Resistance and Inductance of single material vs. layered material

The single conductive material is copper, and the layered material has a thin layer of copper with beryllium on the inside. Resistance shows the expected DC offset achieved when assuming that the resistances of the two materials are in parallel. There is a small offset in resistance across the entire frequency range, and it converges around 100MHz. Inductance converges around 1MHz, and skin depth becomes equivalent to 1mil copper around 5MHz. Below 200KHz, there is a 5% decrease in layered pin inductance. Actual products have a much smaller plating depth than the value assumed here, so the effect of plating was ignored in the remainder of studies.

III. Multi-pin Connectors with Mixed Power, Ground and Signal

With the ever-increasing pin count for signals and the limited board space, high-speed designer sometimes chooses an open pin-field connector for maximum flexibility for carrying both powers and signals. In this section, we will explore the impact of running power through signal in an open pin-field connector and study the crosstalk induced in its neighboring signal. Furthermore, we would like to have some understanding whether board has any impact to the power induced crosstalk.

The test vehicle of this study is a 100mm X 130mm characterization board of APX6 connector as DUT (Figure III-1 and Figure III-2). The board is extracted using Ansys SI-wave while the connector model is simulated by the Ansys HFSS 3D full-wave simulator.

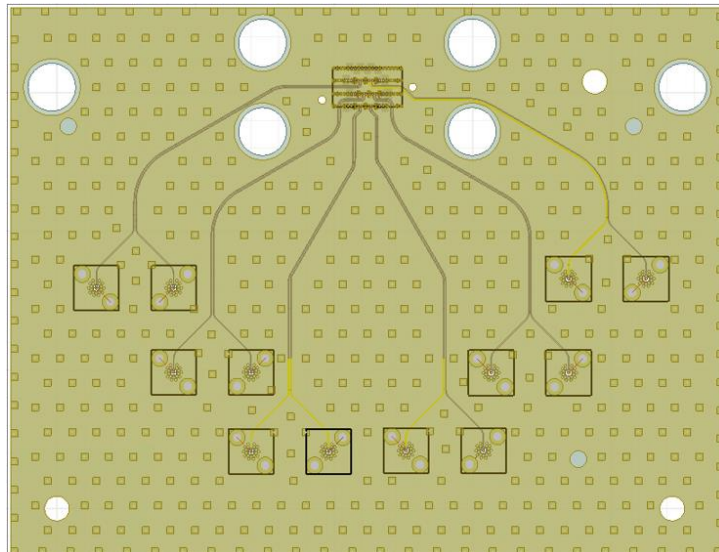


Figure III-1: A 100mm X 130mm test vehicle for an open pin-field connector

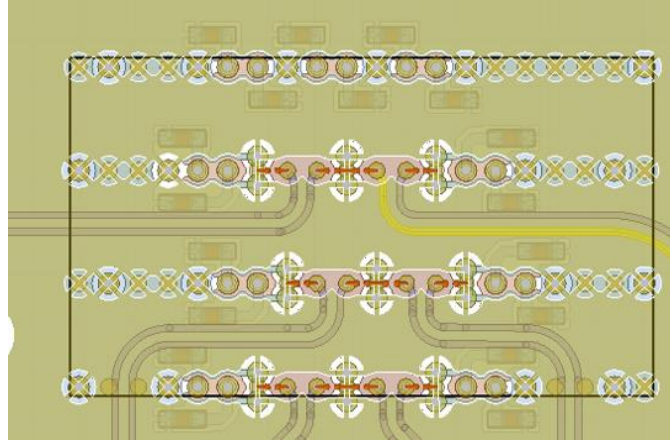


Figure III-2: Breakout region near the BGA pin field

Methodology

To measure the impact of the power induced crosstalk, we apply 1V to the user-assigned power pins (these are normal signal pins) and terminate the user-assigned power pins with 0.1Ω as loading. Ground pins are grounded, and all signal pins are terminated by a 50Ω resistor. Then we observe the nodal voltage at the signal for either near-end or far-end (illustrated in Figure III-3). We verified our setup in ADS, however actual experiment is carried out in Matlab by solving for the nodal voltage as a modified nodal analysis matrix (MNA matrix) for ease of computational convenience.

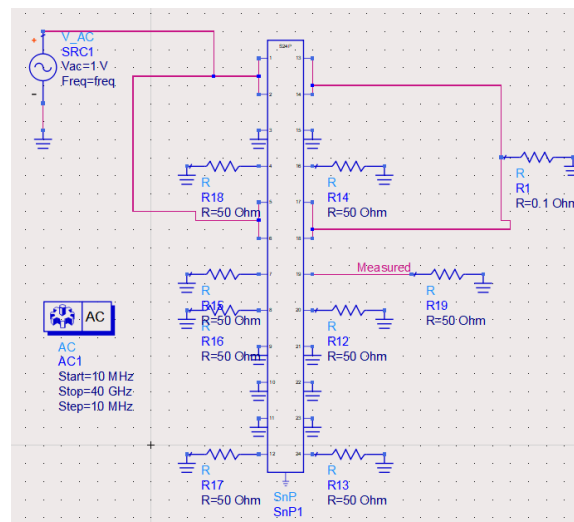


Figure III-3: Test setup for observing voltage at the signal

Pin Assignment Study

We will explore four different pin assignments in an open pin-field connector for powers and signals.

	T	
T	T	
T	T	T
T	G	T
G	G	G
P	G	S
P	G	S
G	G	G
P	G	S
P	G	S
G	T	G
T	T	T
T		T

Figure III-4: Config 1, Power-Ground-Signal

	T	
T	T	
T	T	T
T	G	T
G	P	G
G	P	S
G	G	S
G	P	G
G	P	S
G	G	S
G	T	G
T	T	T
T		T

Figure III-5: Config 2, Ground-Power-Signal

- Config 1, Power-Ground-Signal (Figure III-4)
 - One row is for power, and the next row is for ground, then adjacent row is for signal.
- Config 2, Ground-Power-Signal (Figure III-5)
 - One row is for ground, and the next row is for power, then adjacent row is for signal.
- Config 3, Power bundle (Figure III-6)
 - Bundled the power at a corner and surround ground pins around it.
- Config 4, Power-ground inter-leaving (Figure III-7)
 - Inter-leaving power and ground

	T	
T	T	
T	T	T
T	G	T
G	S	G
S	S	S
G	G	G
G	P	G
P	P	G
P	G	G
G	T	G
T	T	T
T		T

Figure III-6: Config 3, Power bundle

	T	
T	T	
T	T	T
T	G	T
G	G	G
G	P	S
P	G	S
G	P	G
G	G	S
P	G	S
G	T	G
T	T	T
T		T

Figure III-7: Config 4: Power-ground inter-leaving

For the connector-only crosstalk, both near-end and far-end observed voltage is minimal. As one would expected, Config 1 with power further away from signal, it induced less both near-end and crosstalk to the signal (Figure III-8 and Figure III-9).

However, if we measure the voltage with the board, the induced crosstalk gives a very different pattern (Figure III-10 and Figure III-11). First, we noticed that there are harmonic spikes at every ~500MHz. We will investigate this further in subsequent section. Meanwhile, we will focus on comparing the result among these four configurations.

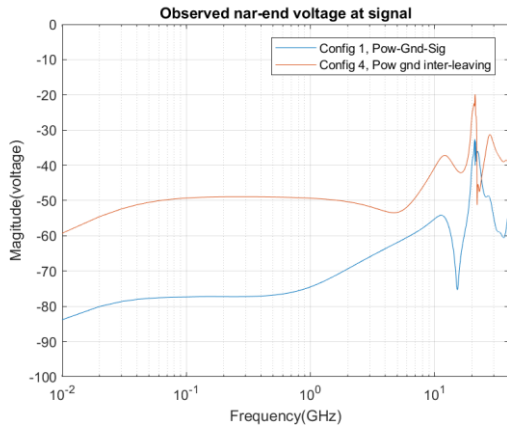


Figure III-8: Observed NEXT for connector only

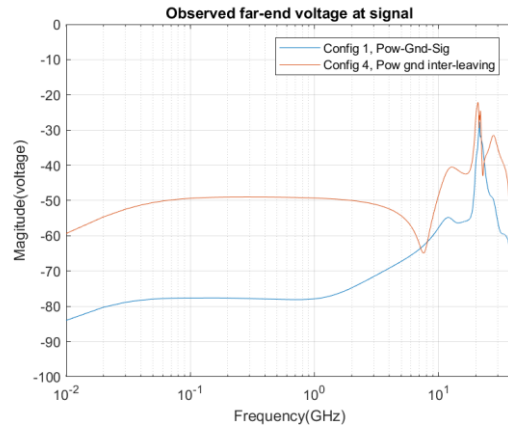


Figure III-9: Observed FEXT for connector only

For Config 1 (pow-gnd-sig), this gives the minimal near-end and far-end crosstalk among all configurations. Config 1 (pow-gnd-sig) and Config 2 (gnd-pow-sig) are almost identical, one would expect Config 1 and 2 to give similar crosstalk since the loop inductance between power and ground row is very similar. However, it turns out that Config 2 gives higher crosstalk (Figure III-10 and Figure III-11). But, why? This is due to the coupling between signal to the power is lower in Config 1 than that of Config 2.

To understand this, we could imagine a 3-conductor system. That will give a 3X3 inductance matrix (Figure III-12). Config 1 and Config 2 corresponds to grounding conductor 1 versus 2 of the admittance matrix (Y). For Config 1, grounding corresponds to zeroing out row one and column one of the 3X3 Y matrix. And for Config 2, grounding corresponds to zeroing row two and column two of the 3X3 Y matrix. Then, we take this reduced Y matrix (becomes a 2X2 Y matrix) and invert it back to give the reduced inductance matrix (2X2). After these operations, if we compare the off-diagonal coupling inductance between Config 1 and 2, we noticed that Config 1 gives smaller off-diagonal value. In short, coupling to the signals in Config 1 (pow-gnd-sig) is smaller than that of Config 2 (gnd-pow-sig).

For config 4 (pow-gnd-inter-leaving), this is one of the favorite pin-out for power integrity engineer because it gives the minimal loop inductance between power to ground. On one hand, this aids power delivery of the PDN on the board or on the package. On the other hand, this gives the highest crosstalk among the four pin assignments because it couples the most to the signal pins. Designer may need to consider the tradeoff between better power delivery and lower power-to-signal crosstalk. If the PDN is good enough, one may avoid the pow-gnd-inter-leaving scheme to minimize the power to signal crosstalk.

Besides Config 1, the next minimal crosstalk pin assignment is Config 3 (power bundle). That means if one could not completely isolate the power to signal by a row of ground, at least group the power pins together and shield it with ground by building a “wall” of ground to shield out the signal pins.

To sum up, if pin-out allow the flexibility to have a complete row isolation of ground, that is the best pin assignment. If not, the second-best pin-out is to group or corner the power pins and surround it with ground pins.

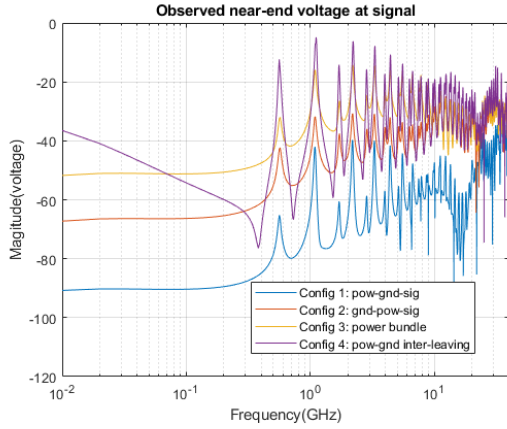


Figure III-10: Single-ended near-end observed voltage measured with the board (Config 1 to 4)

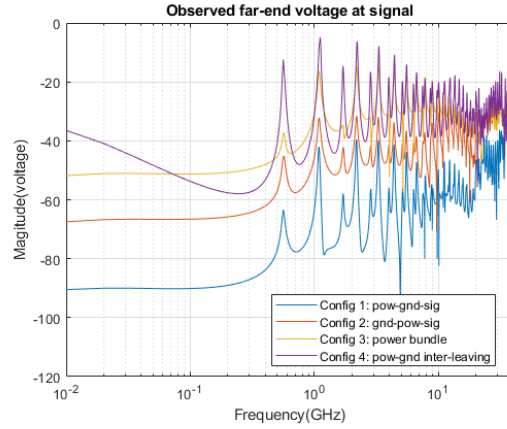


Figure III-11: Single-ended far-end observed voltage measured with the board (Config 1 to 4)

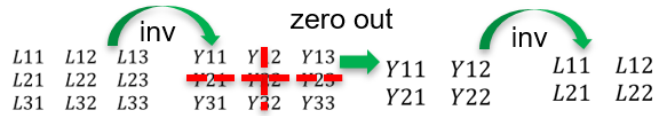


Figure III-12: Illustration of coupling to adjacent rows gives different coupling after grounding

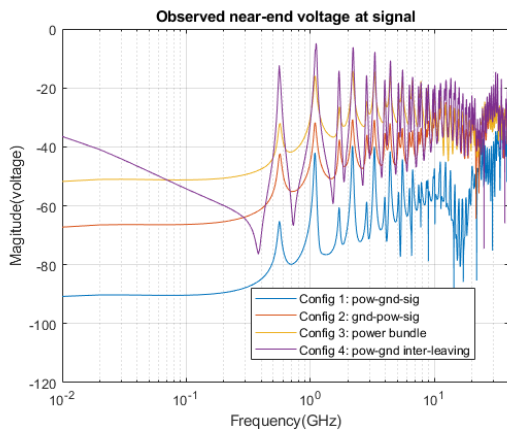


Figure III-13: Single-ended near-end observed voltage measured with the board (Config 1 to 4)

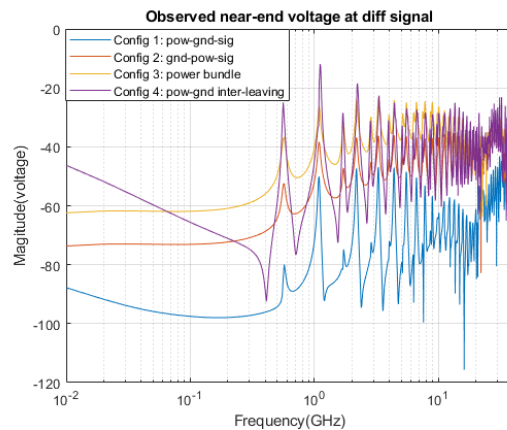


Figure III-14: Differential near-end observed voltage measured with the board (Config 1 to 4)

For differential signal, we noticed that both near-end and far-end give roughly 5-7 dB reduction (Figure III-13 vs. Figure III-14 and Figure III-15 vs. Figure III-16) compared with the single-ended signals. The power induced crosstalk behaves like the common mode noise and differential signaling could alleviate the coupling.

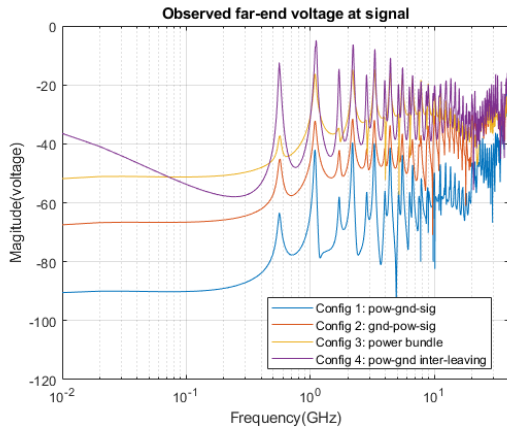


Figure III-15: Single-ended far-end observed voltage measured with the board (Config 1 to 4)

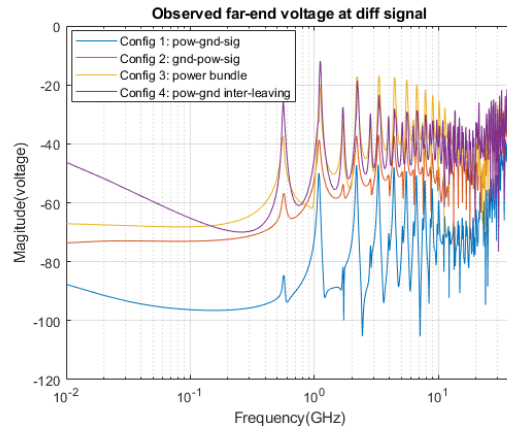


Figure III-16: Differential far-end observed voltage measured with the board (Config 1 and 4)

Simulation and Measurement Correlation

Using Config 3 (power bundle) far-end as an example, measurement with the board confirmed the harmonic pattern observed in simulation. In measurement, the magnitude is more subdued. Nevertheless, simulation tracks measurement of all the spikes although it does not align perfectly in frequency. We will explore further below of the reasoning of the discrepancy.

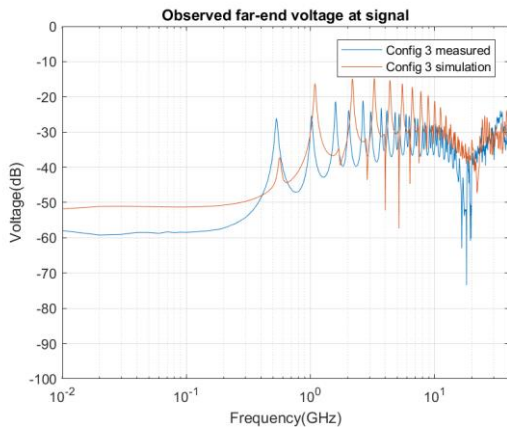


Figure III-17: Correlation of far-end observed voltage measured with the board [linear scale]

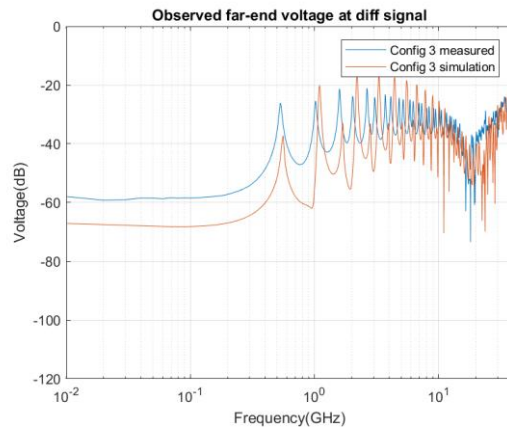


Figure III-18: Correlation of far-end observed voltage measured with the board [log scale]

Investigation of the Spikes in FEXT

To better understand the root cause of the spikes, we compare the crosstalk with a) DUT only (i.e. connector) b) One side of the board without the DUT c) board + DUT + board.

With one side of the board (Figure III-19, orange curve), it already shows the signature like the two boards with DUT—spikes across frequency. The difference is simply lower magnitude. Since the DUT crosstalk is very linear across frequency, the crosstalk with two boards is a level shift from the one side of the board crosstalk. This gives us indication that the source of the crosstalk is coming from the board.

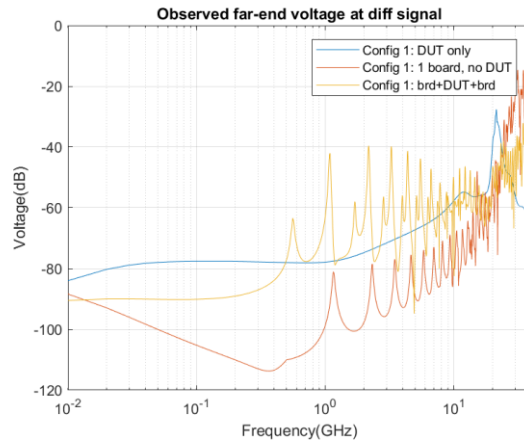


Figure III-19: Test board with ASIC chip

To understand whether these spikes are coming from the plane resonance, we intentionally modified the board and removed the stitching ground via (Figure III-21). We noticed that with or without stitching via, it still exhibits the same signature of giving spikes in FEXT (Figure III-22 and Figure III-23). This shows that this is not likely from plane resonance. Otherwise, with removal of stitching via the resonance should give a different signature.

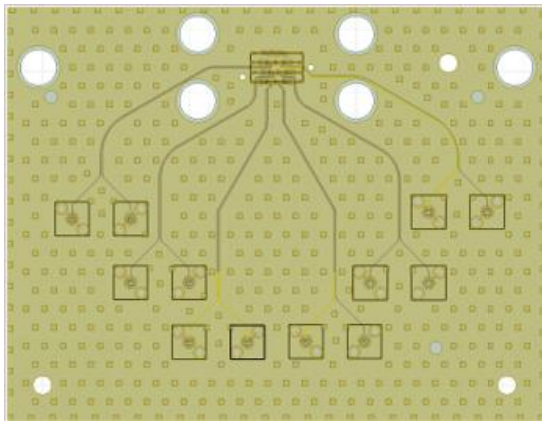


Figure III-20: Original board (with ground stitching via)

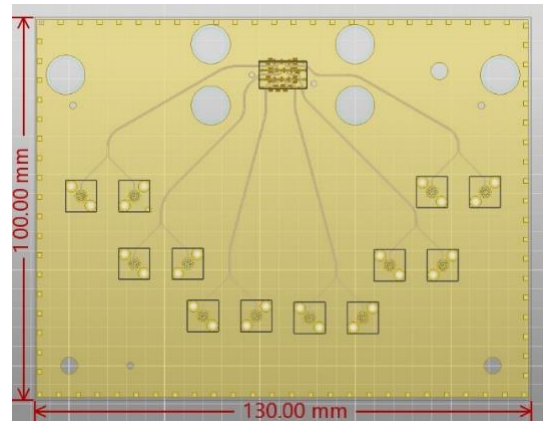


Figure III-21: Modified board with ground stitching via removed except at the edges

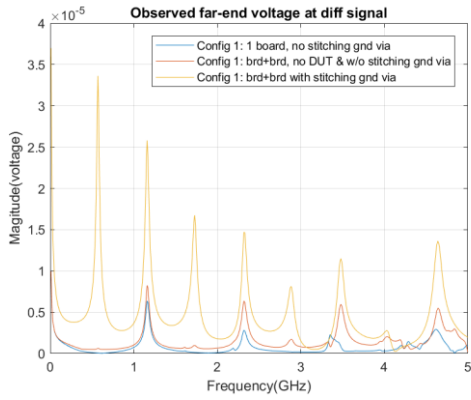


Figure III-22: FEXT with or without stitching via (linear to 5GHz)

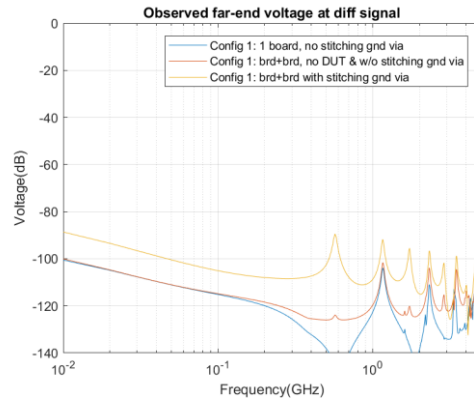


Figure III-23: FEXT with or without stitching via (log to 40GHz).

For further investigation, we reduce the board traces down to just one pair and created three cases for comparison: a) base case one pair, b) 15mm longer trace, c) 15mm longer trace and 30mm larger board by keeping the stitching via at the edge.

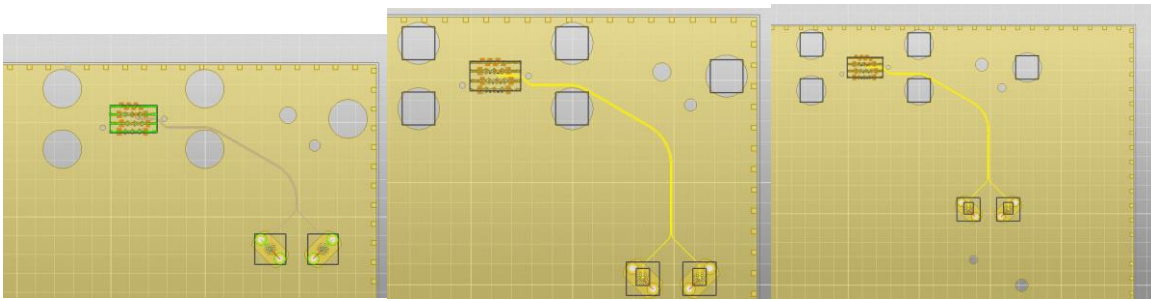


Figure III-24: Left) base case one pair, Middle) 15mm longer trace, Right) 15mm longer trace & 30mm larger board in y direction

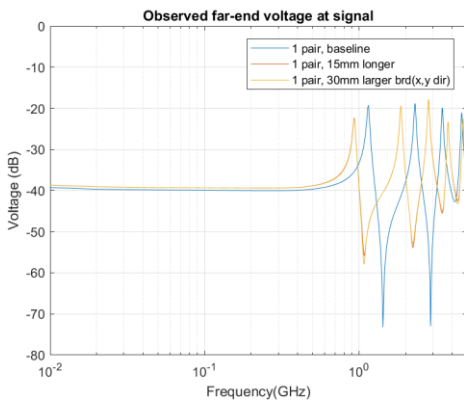


Figure III-25: One pair case comparison

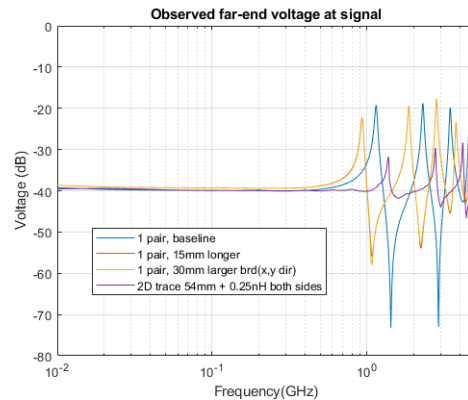


Figure III-26: One pair case comparison and 2D trace with 0.25nH

Comparing with the 30mm larger board case (yellow curve in Figure III-25) with case without the board size change (orange curve), we clearly see that the spikes cannot come from the plane resonance as these two curves are on top of each other. Further, we noticed that the longer trace case (orange or yellow curve) shifts the spikes down compared with the base case. This is simply the result of the longer electrical length and therefore the spikes occur at lower frequency.

So far, we have ruled out the plane resonance. And we observed that with one board the spikes occur. Besides the plane, the bare board remaining component is via. That leads us to further investigate if somehow the via discontinuities will affect the FEXT and result in spike in the board.

We use a 54mm 2D stripline trace and cascade a 0.25nH to both sides to mimic a via. The 0.25nH is approximated by the following formula: $L_{via} \approx 5.08h \left[\ln \frac{4h}{d} + 1 \right] nH$. d is diameter and h is the height. We assume 8mil drill of the via and use 20mil for the length. This gives $\sim 0.25nH$. FEXT of the 2D trace with inductance (purple curve, Figure III-26) gives the same signature as in the board with via. The induced FEXT of a 2D trace (blue curve) in Figure III-28 gives a smooth crosstalk across frequency. However, once the inductances were added to two sides, the spikes show up. Similar trend is observed in S-parameter (Figure III-27), more ripples show up with 0.25nH added.

Going back to the measurement correlation, the discrepancy comes from the via modelling of the board in simulation. Simulation does not give very good return loss correlation compared with measured data and therefore it inadvertently affects the far-end crosstalk correlation. A key takeaway for designer is to minimize reflection discontinuities to ensure resonance-free crosstalk on the board.

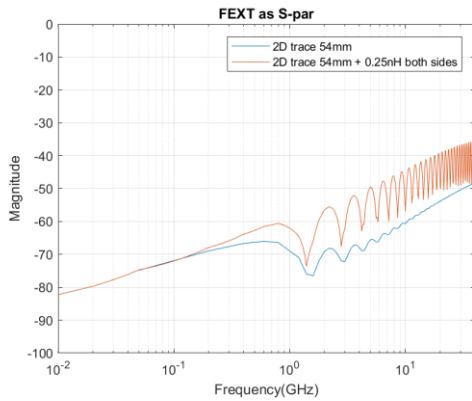


Figure III-27: 2D trace vs. trace + 0.25nH (S parameter)

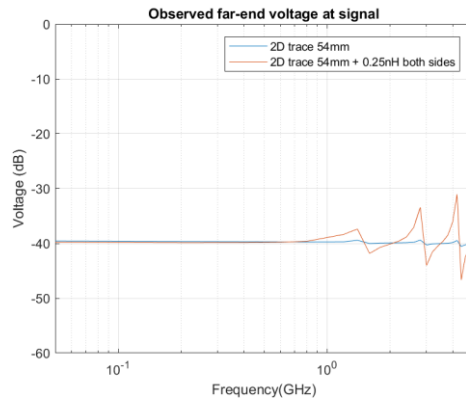


Figure III-28: 2D trace vs. trace + 0.25nH (voltage)

Side Notes on the Metric

In this paper, we adopted the methodology to observe the nodal voltage at the observation point. If the exact same setup (termination and tying the power pins together, Figure

III-31) is simulated and output as S-parameter, the overall pattern looks similar but with more subdued magnitude (Figure III-29 left). One reason could be the S-parameter is assumed to have a reference impedance (50Ω is chosen in the graph) and that makes the result more complicated to interpret. Another subtle point is that if we plot the power sum or linear sum and assume all 4 of those power pins as aggressor, it still does not completely resemble the nodal voltage plot in Figure III-29 right (we do not grounded additional pins in the power sum and linear plot nor changed reference impedance for each individual pin. However, the actual difference is minimal). One of the differences is that before solving for the nodal voltage, the Y matrix is post-processed (think $Yv=I$) because of same voltage at the power pins [combining columns (i.e. $v1=v2$)] and current are distributed among the power pins [combining rows (i.e. $I1=I2$)]. Therefore, the new post-processed Y matrix is not exactly the same as the original one. As a result, simply plotting power or linear sum of the power pin to the victim pin will not show the same result as in the nodal voltage case. However, between power and linear sum, linear sum will resemble better because it sums individual crosstalk term in S. This process is similar to combining the rows in the Y matrix.

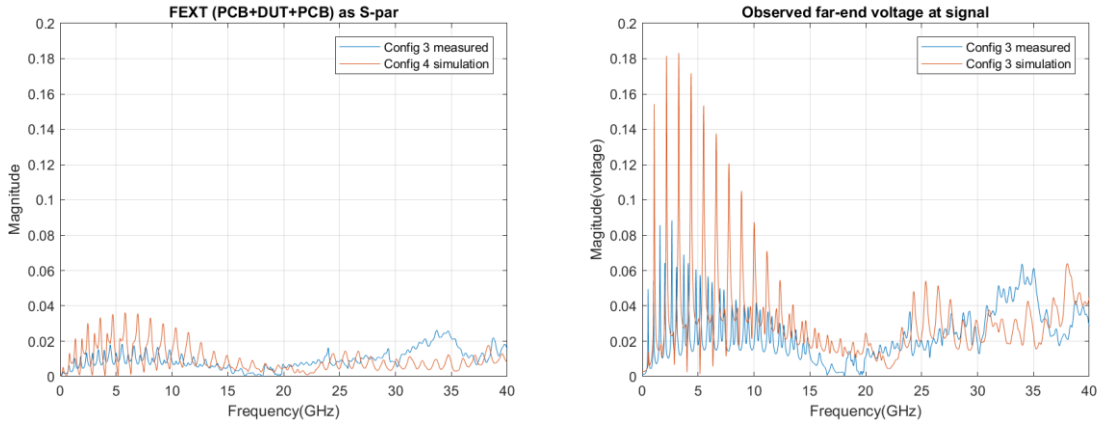


Figure III-29: Observed far-end as S-parameter (left), as nodal voltage (right)

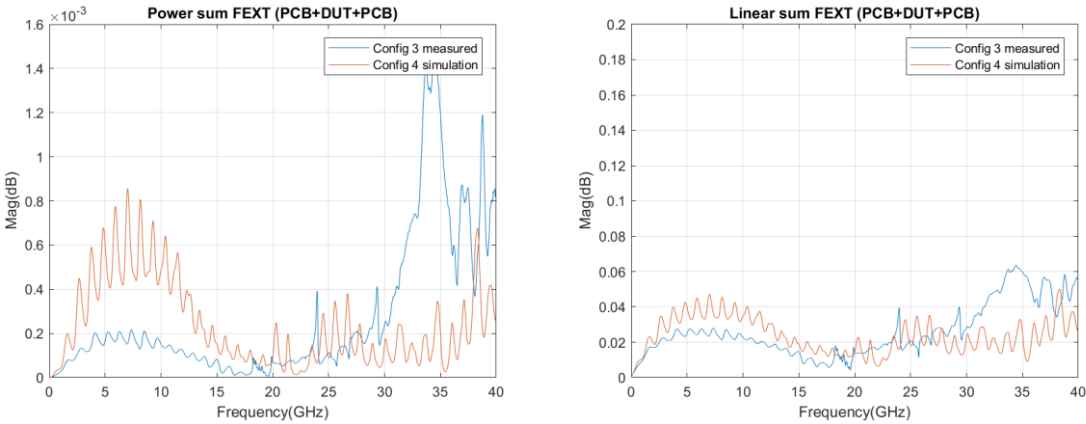


Figure III-30: Observed far-end as power sum (left) and linear sum(right)

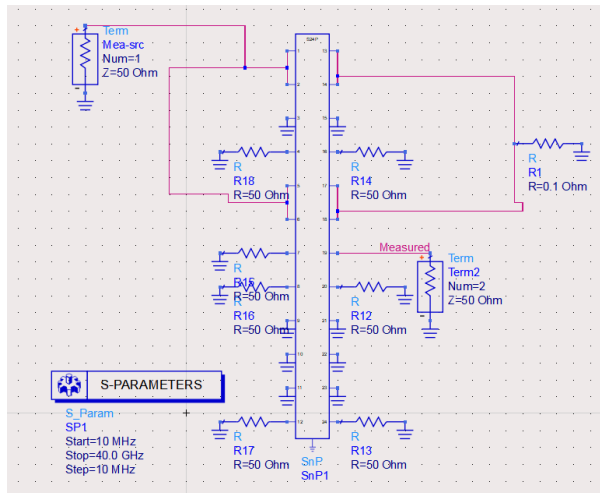


Figure III-31: Setup as S-parameter for output

IV. Impact of User Geometry

To study the impact of current entry and exit directions on the AC performance of multi-blade connectors, simple test boards have been designed with multiple footprints. With the realization that the number of possible permutations with a multi-blade connector due to stackup and layout variants would be overwhelming, a few simple test cases were selected. In Figure IV-1, the layout for three times three variants of a four-blade power connector is shown. On the left, two groups of three footprints are shown for two different variants of the same connector. The upper three footprints are for connectors with mechanical anchor pins; in the lower row of three connectors there are no anchor pins and therefore in tight layouts we can expect an improvement in the spreading resistance and inductance on the printed circuit board. The three layout variants in each row target different pin configurations and escape patterns. The right-most layout groups the adjacent blades into pairs on the same net: two power and two ground blades, with a current-escape path in line with the connector body. The middle footprints also group the adjacent blades into pairs, except the current escape is perpendicular to the connector body. The left-most footprints have one ground blade and three independent power blades, two of them escaping in line with the connector body, the third one escaping sideways. Another part of the test board has a matching set of footprints with the mating parts. Each power net has dedicated test vias to connect instruments. A third triplet of connector footprints is shown on the left of the figure. These footprints take the right-angle version of the four-blade connector bodies and have the same footprints that the other two triplets have.

Figure IV-2 shows a test-board detail for a power-blade signal-pin combination connector. A 4x4 matrix of signal pins is surrounded by a pair of power blades on the North and South of the signal-pin matrix.

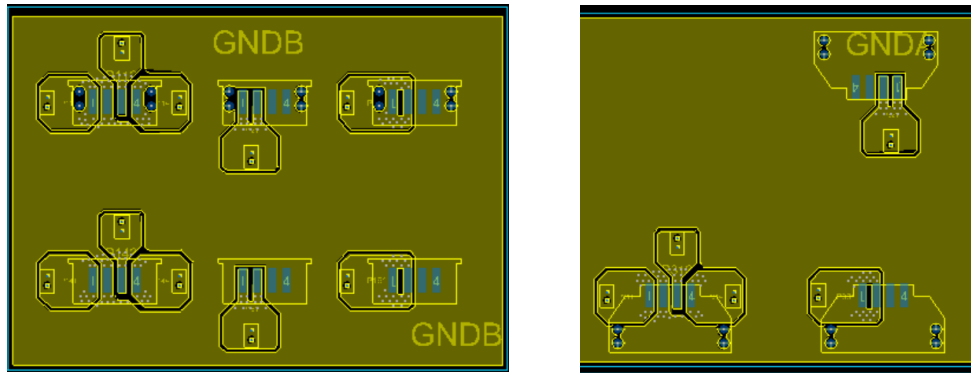


Figure IV-1: Various user geometry for dedicated power blade connector measurement

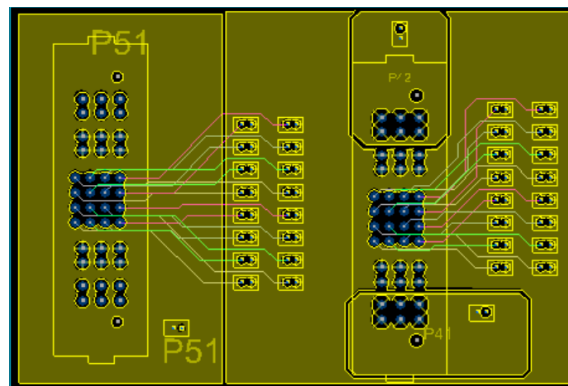


Figure IV-2: Hybrid power and signal connector. Two configurations will be studied.

In this section, we will further explore the impact of user geometry and power and ground assignment effect in a dedicated power blade connector. In addition, we will also investigate a hybrid power and signal connector, and its crosstalk impact to the signals.

Due to the timing of the submission of the paper, the simulation and board measurement work are still work in progress.

V. Measurements and Correlations

Measurement Instrumentation and Setup

Connectors intended for high-speed applications are validated and characterized in custom evaluation boards. The connector pins and their immediate connections to the user geometry are designed for specific impedance, crosstalk and skew targets [3]. This typically means impedance values close to 50 Ohms. Insertion loss (IL) due to absorption losses are usually less important because the connectors tend to be physically and electrically short compared to the connecting traces or cables. The connector itself and the evaluation board as well are designed to minimize reflection losses, crosstalk and skew.

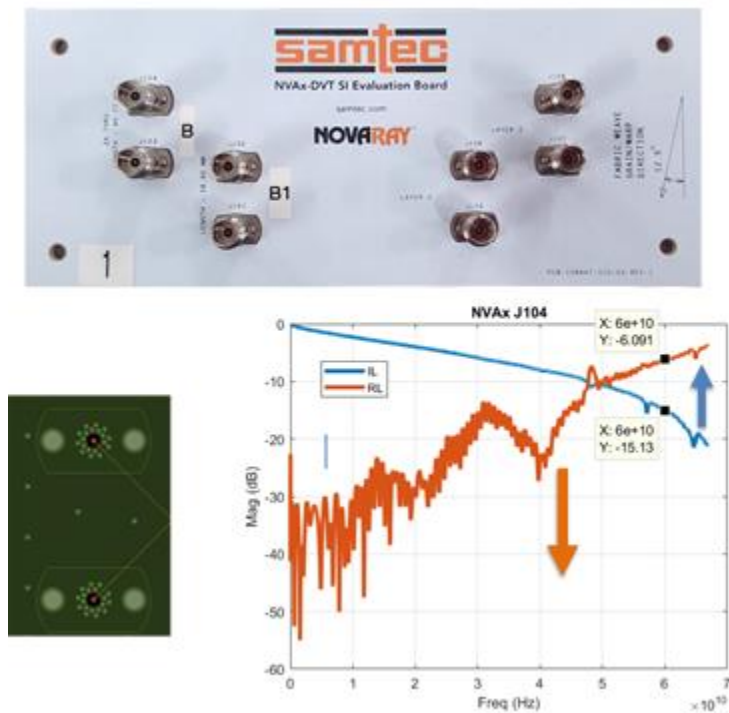


Figure V-1: Evaluation board for a high-speed connector [4].

This also means that the characterization and measurement of a high-speed connector is similar to how we measure high-speed traces and cables, which has well established instrumentation and connection solutions. The quality of the connector can be qualitatively judged from its impedance profile and scattering parameters.

Power connectors, on the other hand, are different. Though matched high-impedance power distribution networks have been proposed, those are not well suited for connectorized applications. Today majority of the power connectors may be optimized for best power transfer, which means lowest possible impedance. Not only the connector pins or blades may have impedances very different from 50 Ohms, even more importantly, the user application geometry tends to have low impedances, sometimes milliohms. For power applications the main parameter to optimize is resistance and inductance; the parallel-path elements of the transmission-line equivalent circuit, capacitance and parallel conductance usually can be neglected. As a result, traditional evaluation boards may not be the best options for power connectors. We need two major changes: frequency range and impedance range. As opposed to high-speed interconnects, power structures have to be measured all the way down to DC. In addition, the measurement range should cover milliohms or less, not tens of ohms. Two-port shunt-through measurement setup is suitable for these purposes [4]. If we want to extend the frequency range to high frequencies, we cannot cover everything with the same instruments and connections. Best is to use multiple instruments and connection techniques, each optimized for specific frequency ranges. As an illustration, we use an evaluation board designed for the high-

speed characterization of a multi-pin connector. Two different instruments [5] and [6] were used with three connection methods to cover the 100 Hz to 40 GHz frequency range.

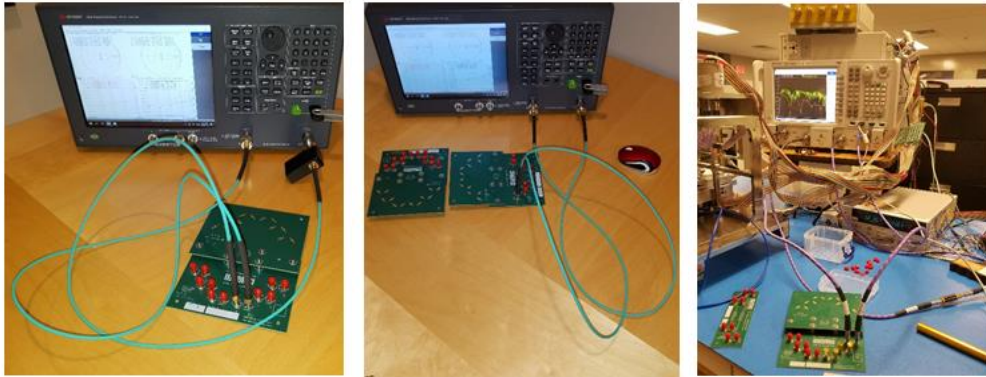


Figure V-2: Measurement setups to cover the 100 Hz to 40 GHz frequency range. Top left: setup used for 100 – 1 MHz. Top right: setup for 1 kHz – 100 MHz frequency range. Bottom: setup used for 10 MHz – 40 GHz frequency range.

These setups use traditional signal-integrity connections assuming that the calibration traces can be used to de-embed the fixture, providing us with the S parameters of the connector itself. A typical measurement result on this evaluation board is shown in Figure V-3.

The figure on the left shows the transfer function magnitude of the calibration trace. Data from the three different instrumentation setups are highlighted by different colors. The blue trace uses a common-mode toroid to eliminate the cable-braid loop error. The orange trace uses the E5061B VNA and runs from 1 kHz to 100 MHz. The green trace starts at 10 MHz and goes up to 40 GHz. Note that there is intentional overlap among the data sets for correlation purposes. We can notice that the green trace approaches its 10 MHz lower end with non-zero gradient. This would be a problem if we used only the green data set: when we calculate the TDR-like response from S parameters, this likely would manifest itself as wrong DC value in the time domain. We can also notice that the three data sets overlap reasonably well and therefore we might wonder why we have to split up the low-frequency range further to two sub-ranges. This will become clear as we look at a crosstalk plot on the right.

Notice that while the blue and green traces blend nicely, the orange trace differs: it does deviate from the other two below 100 kHz. What we see here is the classic cable braid error that we have to take care of in low-impedance power distribution measurements. If we do not eliminate this error, we end up measuring the low-frequency impedance of the two cable braids in parallel. We don't see this error in the through parameters, for instance in S_{21} , because the large useful signal masks out the small voltage drop due to the cable braid. Crosstalk, however, is expected to be zero or close to zero at low frequencies and at that point the cable braid error dominates. In this case a common-mode toroid choke was used that works up to several MHz, but above 10 MHz its performance gradually breaks down. To allow for a decade frequency range of overlap with the high-frequency VNA data, we keep also the data measured with the low-frequency VNA

without the common-mode choke. Note that other solutions to eliminate the cable-braid error are also available, and for instance a wide-band preamplifier can cover the entire 100 Hz – 100 MHz frequency range.

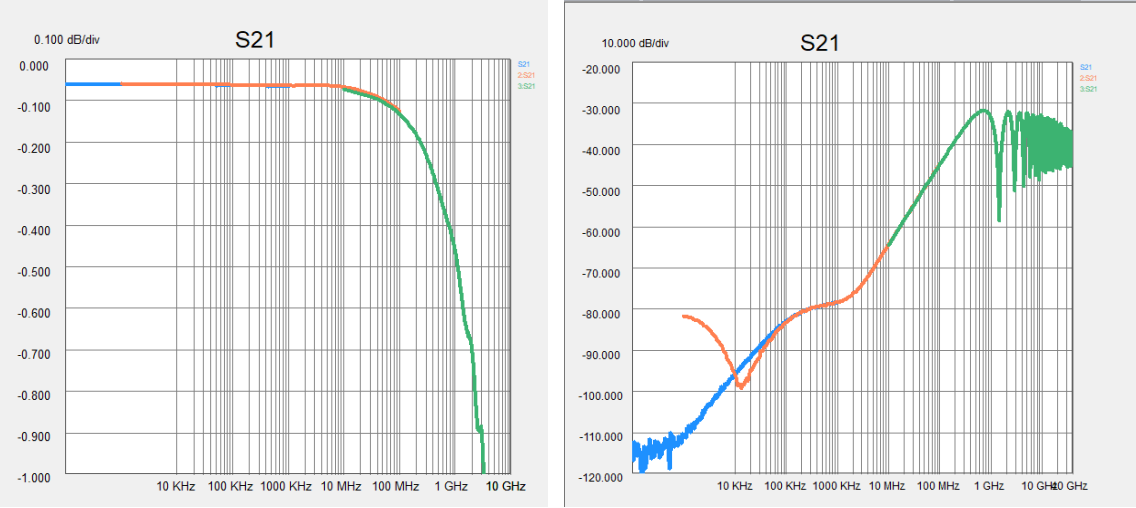


Figure V-3: A through measurement result from the setups shown in Figure 5-2 in the 100 Hz – 40 GHz frequency range. On the left: through measurement; on the right: near-end crosstalk

Measurement results on stand-alone connectors

Due to the limited time available, we wanted to use existing signal-integrity evaluation boards as much as possible. Power connectors usually have test boards to check DC current-carrying capability and contact resistance, but not well suited for AC measurements. On the other hand, while high-frequency miniature connector pins cannot be easily measured by hand-held probes, the power connector blades tend to be big enough in size that manual measurement without fixtures are doable. Figure V-4 shows a small multi-blade power connector.

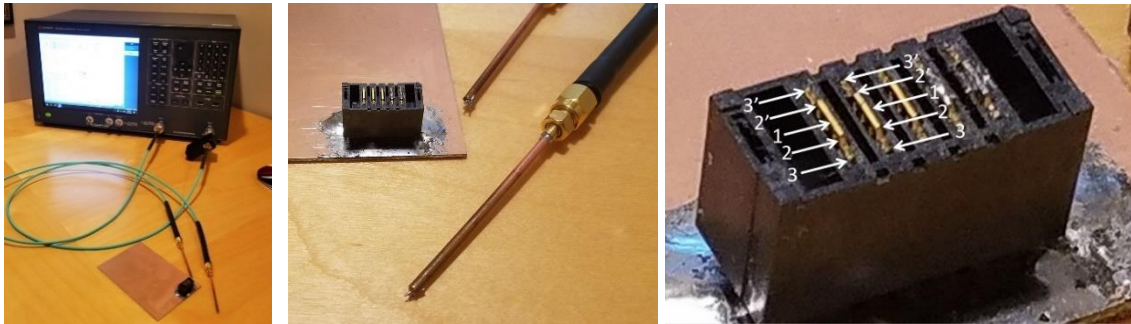


Figure V-4: Measurement setup for blade connector with connection points shown on the right

The socket side was soldered down on a solid copper sheet and blades on the open top of the plug were probed with handmade semirigid probes. The solid copper sheet connects all socket blades together and therefore this arrangement allows us to measure the loop impedance of mated blades at low frequencies. The same common-mode choke that is shown in Figure V-2 was used to reduce the cable braid error. To further suppress the cable-braid error, 0.5-meter flexible cables with low braid resistance were used [7].

Measurements were taken in different configurations. The sketch on the right of Figure V-4 shows the connection points used. The impedance magnitude as well as extracted resistance and inductance for the tested configurations are shown in Figure V-5 and Figure V-6.

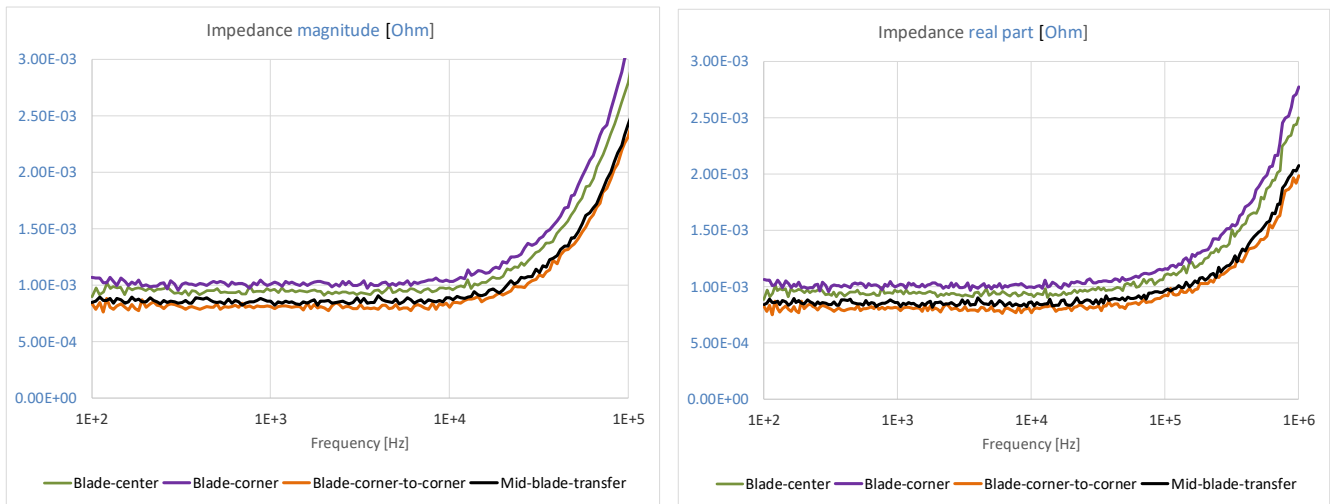


Figure V-5: Impedance magnitude on the left, extracted resistance on the right for the configurations tested in the setup shown in Figure V-4.

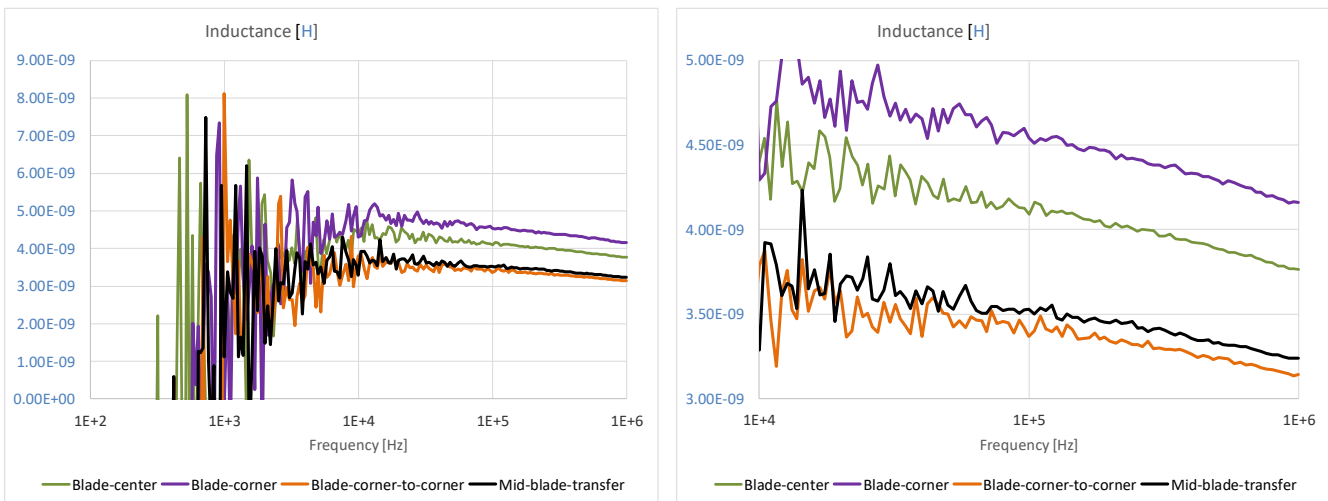


Figure V-6: Extracted inductance on the right for the configurations tested in the setup shown in Figure V-4. Full measured band on the left, zoomed scale on the right

The reference measurement result showing the parasitic limit of the probe setup is shown in Figure V-7. Placing both probes on a solid copper sheet, the residual reading is around 0.4 mOhm and 120 pH. Though the reading is a little noisy, it could have been made lower noise by lowering the IF bandwidth of the instrument. For this particular setup and setting, the noise floor was approximately ten times lower in impedance magnitude reading. The non-zero resistance and inductance is associated with the finite distance between the probe tips and the finite conductivity of the shorting sheet.

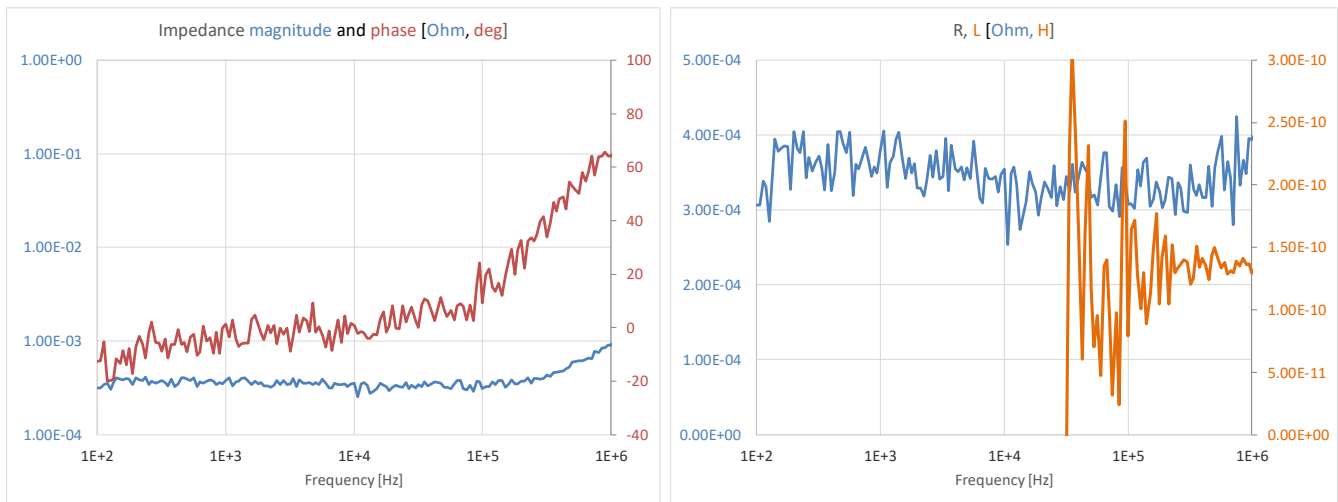


Figure V-7: Parasitic limits for the test setup used for Figure V-5. Real part of impedance and extracted inductance when the probes touch down on solid conducting surface

Field-solver simulations [8] were made to get correlation data on some of the measured configurations. Figure V-8 shows some of the connection geometries that were tried and used. Figure V-9 shows the correlation.

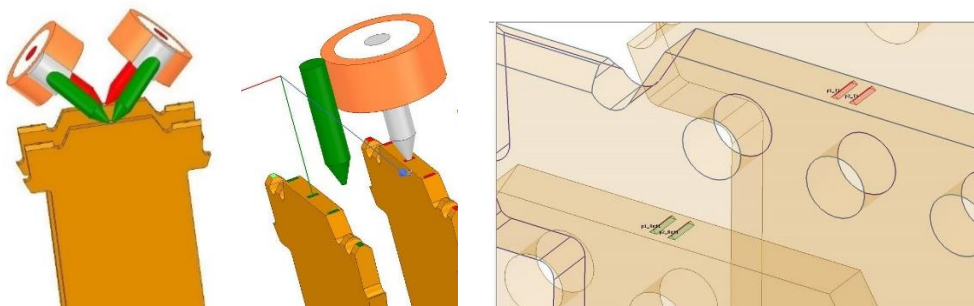


Figure V-8: Some of the geometries simulated in Ansys HFSS and Q3D

To match the Two-port Shunt-through measurement geometry, one set of simulations used two short sections of coaxial cables with 40-mil pigtail connection to the target. The left sketch in the figure shows the two probes measuring the self impedance at the center points of adjacent blades, while the other ends of the blades are shorted together. While in

measurements of low impedances we need the two-port connection, it is not necessary in simulations. This was tested in a setup similar to the sketch in the middle of the figure. On the right of the figure the lumped Circuit Port is shown in the form of small triangular add-on features. The circuit port is considered as non-ideal and the tool vendor cites formulas describing the port inductance and resistance. The one-port connection was quickly ruled out due to its very high sensitivity of deembedding parameters to any small geometry changes. Simulations with the Two-port Shunt-through connection correlated reasonably well at higher frequencies, but below 1MHz it did not report any resistance or inductance measurement. However, even with solving inside the metal, frequency dependent change was not seen below 1MHz. The most detailed correlation was obtained with Circuit Port.

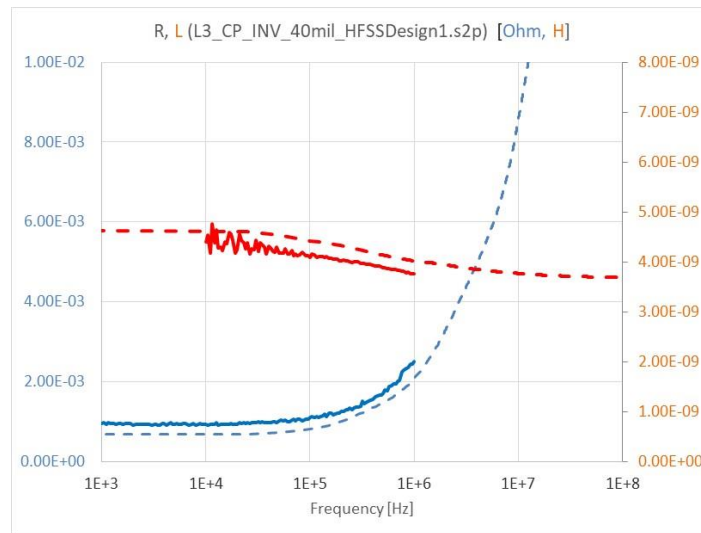


Figure V-9: Correlation between measured and simulated loop resistance and loop inductance in the geometries shown in Figure V-8; on the left: test points at the center of blades; on the right: test points at the corner of blades. Solid lines: measured; dashed lines: simulated

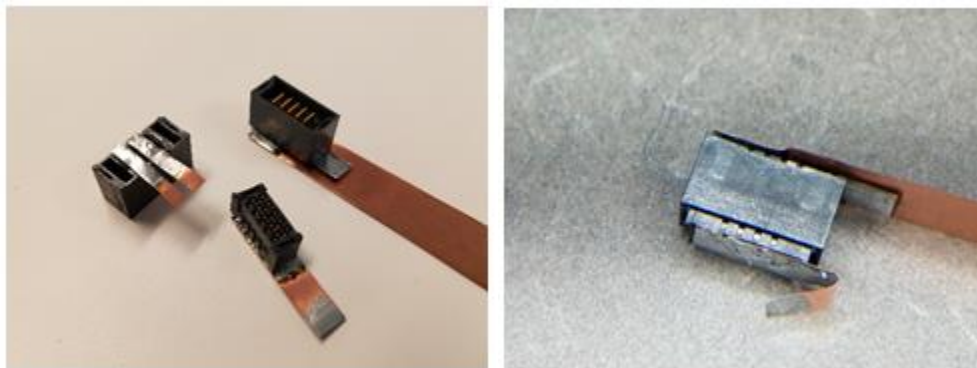


Figure V-10: Additional geometries tested on the blade connector. A) On the left two and two adjacent blades brought out sideways with metal strips. On the top right: two and three blades grouped, brought out longitudinally with isolated copper strips. Bottom: Socket with shorted blades. B) Close-up of the configuration from the top right in A)

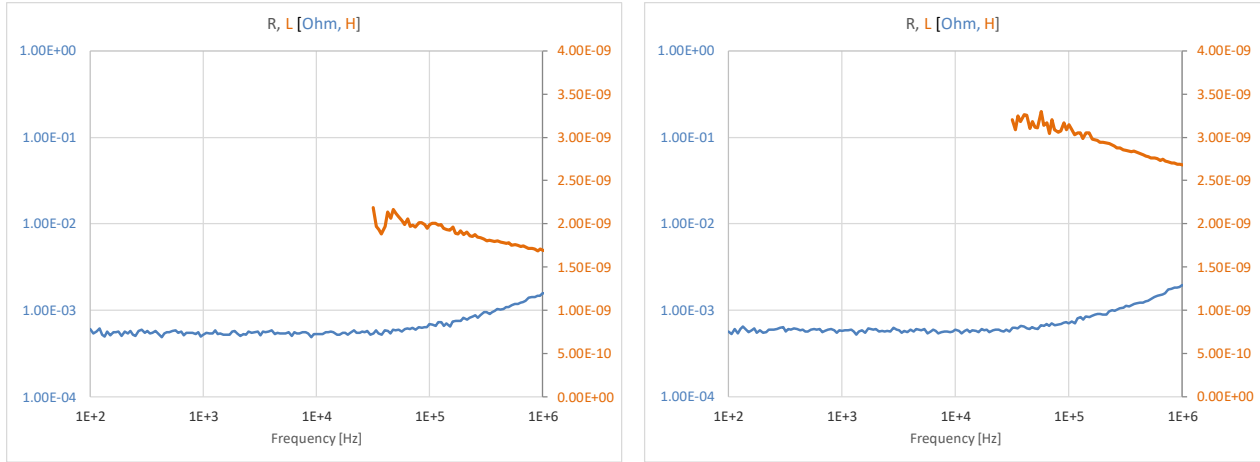


Figure V-11: Loop resistance and inductance of a 5mm stack height connector. On the left: adjacent blades. On the right: second-neighbor blades

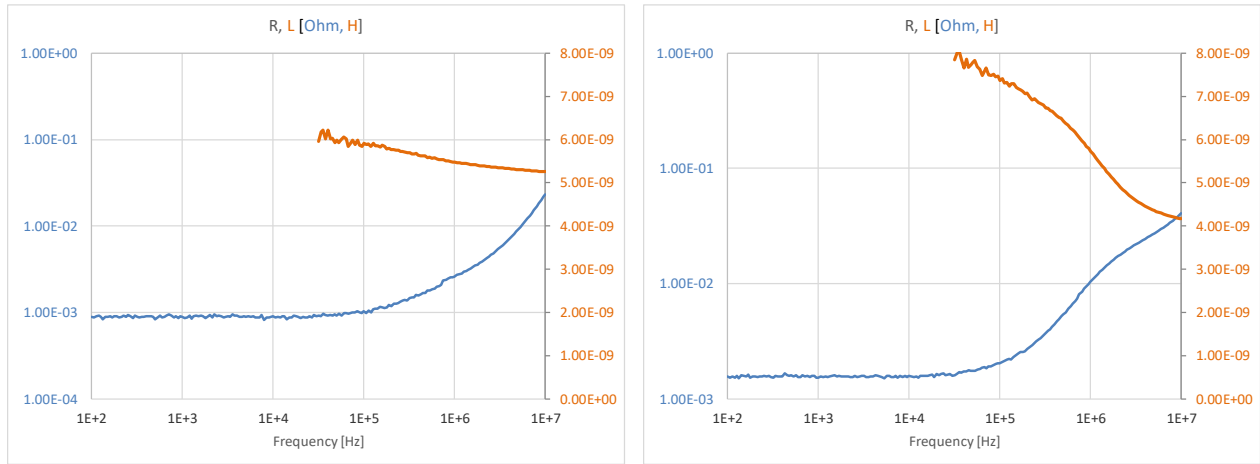


Figure V-12: Loop resistance and inductance of a 12mm stack height connector. On the left: two blades, second neighbors. On the right: two and three blades are tied together with metal strips exiting the connector body longitudinally

Simulation to Measurement Correlation with De-embedding

The connector characterization board was measured with 2 different VNAs with three setups whose combined frequency data ranged from 1 kHz to 40 GHz. The three setups and the test board were shown in Figure V-2. The three data sets were combined into a single data file and then the calibration traces were de-embedded to extract the raw connector parameters. In Figure V-13 and Figure V-14, the insertion loss, resistance, and inductance are compared to the simulated results of the same connector.

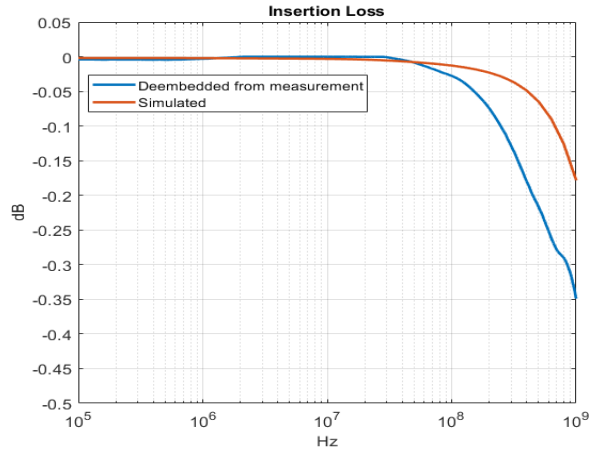


Figure V-13. Simulated vs. De-embedded Connector Insertion Loss

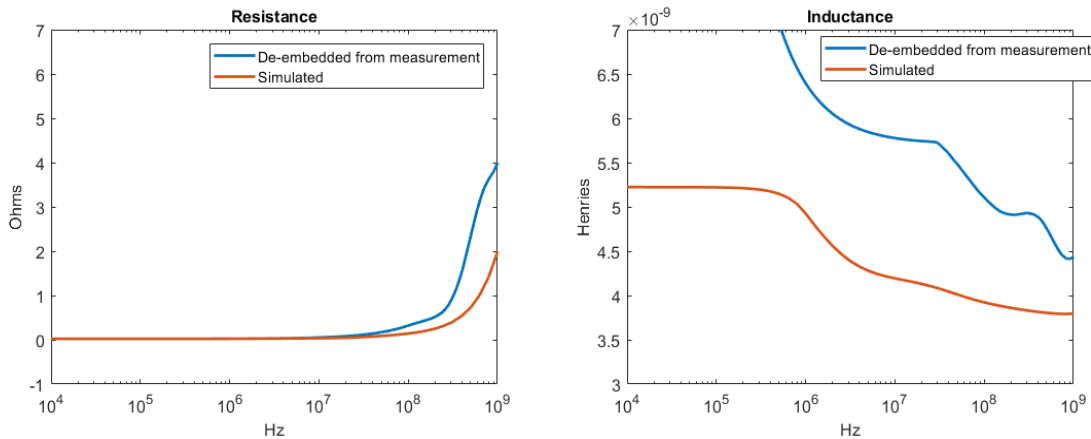


Figure V-14. Simulated vs. De-embedded connector resistance and inductance

The de-embedded results for resistance and insertion loss basically mirror each other. There is more resistance in the de-embedded data, but the trend vs. simulation is very close. For inductance, the de-embedded data is problematic below 1MHz, but this is the region where simulations show roughly constant inductance due to skin depth. Beyond 1MHz, it trends very close to the simulated data with around 0.5 – 1.0nH offset.

The de-embedded results have obvious accuracy issues, primarily due to the fact that the test board was created for high-speed validations and as such the board traces are electrically much longer than the connector. However, they are close enough to the simulated results to conclude that the 3D simulator can produce accurate resistance and inductance models even at low frequency.

VI. Summary and Conclusions

In this paper we showed simulation and measurement solutions needed to characterize multi-pin connectors for power application. It was shown that the Two-port Shunt-through connection scheme is mandatory in measurements, whereas in simulations it is necessary only if there is large mode conversion. The Two-port Shunt-through connection was challenging in some cases. Single-port simulations, on the other hand, were very sensitive to small changes in the port that had to be deembedded. The best correlation was found with Circuit Ports, which captured currently the low-frequency resistance and inductance change.

Acknowledgement

The authors wish to thank Scott McMorrow of Samtec, Jim DeLap of Ansys, David Michaud of Samtec, and Jean-Remy Bonnefoy of Samtec for their valuable comments, help and support.

References

- [1] "Current Gradients in Power Delivery," DesignCon 2017, Santa Clara, CA
- [2] Effective Resistance and Inductance of Iron and Bimetallic Wires, Bulletin of Bureau of Standards, April 14, 1915.
- [3] Blando, Ballou, McMorrow, "Increasing Broadband Interconnect Characterization," EDICON 2018, October 17-19, 2018, Santa Clara, CA
- [4] "Accuracy Improvements of PDN Impedance Measurements in the Low to Middle Frequency Range," DesignCon 2010, http://www.electrical-integrity.com/Paper_download_files/DC10_12-TH3_Novak-Mori-Resso.pdf
- [5] N5227 Vector Network Analyzer, Keysight, <https://www.keysight.com/en/pdx-x201878-pn-N5227A/pna-microwave-network-analyzer-67-ghz?nid=-32497.1150218.00&cc=US&lc=eng>
- [6] E5061B Vector Network Analyzer, Keysight, <https://www.keysight.com/en/pdx-x201771-pn-E5061B/ena-vector-network-analyzer?cc=US&lc=eng>
- [7] "What Makes PDN Cable Special," SI Journal, November 12, 2019, <https://www.signalintegrityjournal.com/blogs/8-for-good-measure/post/1441-what-makes-pdn-cable-special>
- [8] Ansys High Frequency Structure Simulator, <https://www.ansys.com/products/electronics/ansys-hfss>