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224Gbps-PAM4 End-to-End Channel Solutions for High-Density Networking System

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Abstract

In this paper, the 224Gbps-PAM4 channel solutions for high-density networking system are explored. The signal integrity design challenges are analyzed, and the key enablement solutions are proposed. These challenges include how to breakdown the link budget among the system components of package, board, cable, and connectors, and how to design these components within their respective loss budgets. Package design needs to consider higher-order mode propagation and dispersion, plane resonance, transmission loss, cross talk, vertical transition, and BGA ball pitch and ball pattern. PCB requires a careful architectural design of channel placement, trace breakout/break-in and via optimization to address the horizontal and vertical loss, via-to-via and trace-to-via coupling, especially when dealing with the small ball pitch high-density board design. An accurate broadband package-PCB co-modeling methodology is essential to an efficient system co-design and is also introduced in this paper. A good correlation of the integrated package-PCB model vs. cascaded package and PCB models can be achieved in the frequency range of DC-80GHz. Moving to 224Gbps-PAM4 from 112Gbps-PAM4, the existing cable assembly and connector mating interface design may become a gating factor due to the limitation of the backward compatibility, and the innovation design of the cable and connector will give more margin to the system. Amongst all these design challenges, the transmission loss is the greatest one that PAM4 signaling encounters. In this paper, we proposed a feasible/realizable loss budget for package, board, cable, and connector for a high-density networking system application that includes up to 512 lanes operating at 224Gbps-PAM4 data rate per lane and targets a total end-to-end (bump-to-bump) link budget of ≤ 40dB at Nyquist frequency. The package and board enablement solutions, as well as the cable assembly forward looking opportunities are explored to meet the loss target.

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Jenny Xiaohong Jiang is a Principal Engineer at Intel Corporation. She has over 20 years of package and board design experience in high-speed transceiver and mixed-signal design. She has 11 issued patents and over 30 journal and conference publications at DesignCon, ECTC, IEEE-IMS. She has served as Panelist, session chair and invited speaker to many industry conferences.

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Ed Milligan is the Senior Director of the Programmable Technology and Systems Engineering Group at Intel. His team's focus is on package technology, design, Signal Integrity, Power Integrity, and platform power delivery. He holds two patents and over his 27-year career he has designed or managed design teams delivering Analog/Digital (Mixed Signal) PHYs/Transceivers such as DDR, PCIe, HBM, SONET, Ethernet and high speed in package die to die interconnects.

Yee Lun Ong is a Signal Integrity design lead with Intel PTSE (Programmable Technology and System Engineering) Group in Penang, Malaysia. He has 9 years of package and board design experience with focus on HSSI and PCIe.

John Medina is a Package Design Engineer with Intel PTSE (Programmable Technology and System Engineering) Group. He has over 30+ years of extensive experience in PCB/Package design and Co-designs, providing training and preforming Signal integrity analysis using state of the art Cad Tools.

Qian Ding is a packaging R&D Engineer with Intel PSG. She holds an MS degree from UC San Diego on Analytical Electromagnetics. Her current focuses include high-speed 2.5D interconnect modeling and Package architecture pathfinding.

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Stas Litski is a team leader of the Signal and Power Integrity team at Intel Analog Mixed Signal division, responsible for development, design, simulation and measurement of package and boards for validation of next generation Intel HSIOs IPs such as 112Gbps and 224Gbps.

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Introduction

Next generation data networking system requires combination of high bandwidth at faster data rate to maximize the system throughput. Current 50T switch system with 512 lanes running at 112Gbps will double the capacity to 100T if the data rate increases to 224Gbps. PAM4 signaling has been widely adopted due to below described advantages: 1) Transistor and process node can be scaled to PAM4 baud rate; 2) Better SNR performance when the SERDES can support PAM4 bandwidth; 3) PAM4 is more efficient and simpler in coding scheme than PAM6, therefore requires less power and area; 4) Backward compatibility to 112Gbps; 5) Optical link operating with PAM4 also prefers PAM4, hence compatible electrical and optical signaling for better power and cost in the host-to-host link with optical medium. 224Gbps-PAM4 signaling, however, faces more challenges of bandwidth in the electrical channel design. It is observed that when the operation frequencies exceed 45GHz, the electrical performance of most passive components drops off considerably, and the traditional design can hardly meet the 224Gbps system requirements. The already challenging electrical requirements of high bandwidth are further complicated by the consideration of high SERDES I/O density.

In this paper, the signal integrity design challenges of 224Gbps-PAM4 networking system are analyzed, and the key enablement solutions are proposed to meet the end-to-end (E2E) loss budget of ≤40dB. The link budget requires a reasonable distribution among the bi-direction package, board, cable, and connectors. In this paper we will describe how to breakdown the link budget among the system components and how to design these components within their respective loss budgets.

Package design needs to consider higher-order mode propagation and dispersion, plane resonance, transmission loss, cross talk, vertical transition, and BGA ball pitch and ball pattern. Desired next generation package trace loss target for interpretation flexibility is 0.123 dB/mm at Nyquist frequency to allow up to a total of 60mm (TX+RX) package trace routing. This can be achieved through a.) skip-layer trace routing; b.) use of low loss material; c.) advanced copper surface treatment for smooth surface roughness. Package vertical loss target is 1dB. This requires ≤0.8mm BGA ball pitch and < 1mm package core thickness. Thick core will introduce dramatic loss beyond 60GHz. Small BGA ball size can further reduce package discontinuities and package loss. A 224Gbps-PAM4 package design practice was described in our 2021 DesignCon paper [1] that used 0.5mm BGA ball pitch. This paper discusses the 0.8mm ball pitch package and PCB design to address the large-formfactor package reliability concerns.

PCB design requires a careful architectural planning for the channel placement, trace breakout/break-in and via optimization to minimize the horizontal and vertical loss, and the via-to-via and trace-to-via coupling, especially when dealing with the small ball pitch high-density board design. Via coupling due to the deep BGA row arrangement in the high-IO count board design requires novel via configuration to diminish both the trace-to-via and via-to-via coupling. Via stub length significantly impacts the PCB loss beyond 45GHz and should be controlled to be < 6 mils in the 224Gbps-PAM4 board design. A desired next generation PCB trace loss target for interpretation flexibility is 0.95 dB/inch at Nyquist frequency in the global routing area to allow up to a total of 10-inch (TX+RX)

PCB trace routing. This can be achieved through the skip-layer trace design and use of ultra-low loss material as well as HVLP copper surface treatment for a smooth copper surface roughness. PCB skip-layer trace routing requires more routing layers and therefore a deeper via transition. PCB via vertical loss should not exceed 1dB when the via is connected to the longest trace. This requires the via length to be less than 65mils and the via stub length smaller than 6 mils. Well-controlled variations of the dielectric material properties, dielectric thickness and copper geometry are also important for a successful design. A 224Gbps-PAM4 PCB breakout design practice was described in our 2021 DesignCon paper [1] that utilized 0.5mm BGA ball pitch for FPGA applications. Similar optimization methodology was leveraged in the 0.8mm ball pitch channel breakout and via transition design.

The package and PCB are often designed separately, and the optimized package and PCB models are then cascaded for performing a link simulation. The BGA ball is included in the package model and should not be double counted in the PCB model. How to terminate the PCB ball pad is critical for an accurate PCB modeling. In this paper, a coax port at the package-PCB interface is designed that accurately captures the pad capacitance yet not introduces any artificial discontinuities. The cascaded package and PCB models are well correlated with the integrated package-PCB model in the frequency range of DC-80GHz.

Several cable/connector configurations were investigated, and it is believed that due to the backward compatibility limitation, the projected cable assembly loss target based on current cable and connector characteristics is ~ 15dB (1m cable + 2 connectors). The cable assembly design is not within the scope of this paper, however, with some technological breakthroughs and the well-controlled manufacturing tolerance, the 1m cable + 2 connector configuration should target to meet ~ 10 dB loss target to the Nyquist frequency. An example of the connector mating interface optimization is described in this paper that showed 3.2dB loss improvement in a cable assembly with 2 connectors.

The above stated approaches drive the key enablement solutions to a successful 224Gbps-PAM4 high-performance and high-density system design.

224Gbps-PAM4 Link Budget and Breakdown

High-speed SerDes interface serves as a fast and reliable external connectivity between semiconductor chips. Connection length in the chip-to-chip or chip-to-module applications is less of a concern at 224Gbps data rate and PAM4 modulation is widely adopted. However, a lot of high-density data center network connection requires a 7 to 12-inch (TX+RX) PCB trace routing with 1-meter cable and two connectors. This long-reach channel is very challenging with PAM4 modulation. On the other hand, common modulation across all the reaches enables the compatibility and lower cost and power for the ecosystem. Therefore, how to address the signal integrity challenges of a long-reach

electrical channel using PAM4 modulation yet with reasonable power consumption becomes very important.

In this paper, a 40dB end-to-end link budget at 53GHz is proposed, and a loss breakdown is analyzed for package, PCB, and cable assembly.

Figure 1 shows the channel topology and the loss breakdown. The investigated channel consists of a bi-directional IEEE standard package of 30mm (one way) trace length, a high-density board of up to 10-inch TX+RX routing length, a 1-meter cable with two connectors.

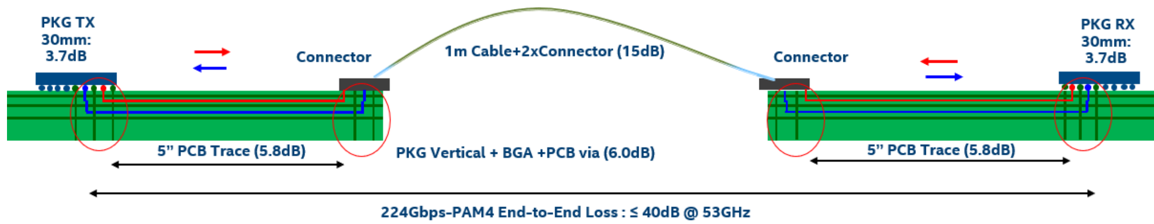

Fig. 1. Channel topology and loss breakdown among package, board, and cable/connector.

Table I summarizes the link budget analysis as well as the constraints and enablers of each component for meeting the 40dB end-to-end loss target up to 53GHz.

Components	Package Trace	Package Vertical	PCB Trace	PCB Vertical	Cable+2x Connector	Total Loss @ 53GHz
Loss Characteristics	0.123 dB/mm (Avg)	1 dB	0.95 dB/inch (Global) 2.4 dB/inch (BO)	1 dB	15 dB	40 dB
Enablers/ Constraints	Low loss material Smooth Cu Skip layer trace ≤ 60mm trace length (TX+RX)	≤ 0.8mm ball pitch ≤ 1050 um core ≤ 22 Layers	Ultra low loss material HVLP Cu Skip layer trace ≤ 10-inch trace length (TX+RX)	≤ 65 mil via length < 6 mil via stub ≤ 8 signal routing layers	1m Cable	

Table I. Link budget analysis and key component enablers.

A ≤0.8mm BGA ball pitch is essential to eliminate the higher-order mode propagation in the package and board for 224Gbps-PAM4 signaling. Package trace loss estimate is based on Intel advanced substrate material and combination of skip-layer [2] and regular trace routing. The average package per-unit-length loss capability depends on the proportion of the skip-layer trace length in the whole trace routing and can be adjusted. PCB trace loss estimate is based on Megtron-8 equivalent PCB material and combination of skip-layer and regular trace routing. A smooth copper surface roughness is critical in reducing the conductor loss. In the package design, it is required that the package core thickness be less than 1000um and no more than 22 total routing layers (~ 25um buildup thickness is assumed) be used to meet the 1dB package vertical loss target. For PCB design, the optimized PCB configuration should be able to accommodate up to 8 signal routing layers with controlled maximum via length to be less than 65mils and via stub length smaller than 6mils to meet the 1dB PCB vertical loss target. Cable assembly loss budget is 15 dB with a 1-meter cable and 2 connectors.

The described link budgeting can be applied to guide the PCB routing length planning toward an end-to-end loss target, as shown in Figure 2, where an IEEE 802.3 reference package of 30mm trace length each way and a 1-meter cable with 2 connectors are utilized.

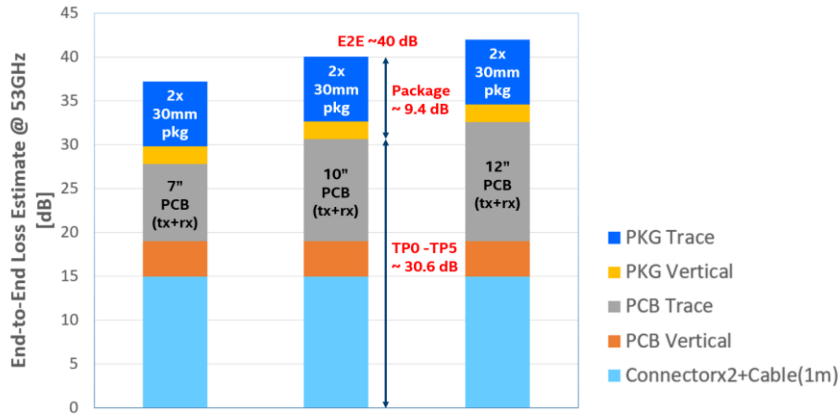

Fig. 2. Link budgeting for different PCB routing length at 53GHz (IEEE standard package of 30mm trace length each way and 1m cable with 2 connectors are assumed).

224Gbps-PAM4 Channel Characteristics and Solutions

Based on the link budget and the loss breakdown analyzed in the previous chapter, the designed channel characteristics are verified, and the electrical performance, as well as the channel model topologies are demonstrated in Figure 3 to Figure 7. Package and PCB design enablement and co-modeling methodology are described in the subsequent chapters, followed by a forward looking of the next generation cable assembly features.

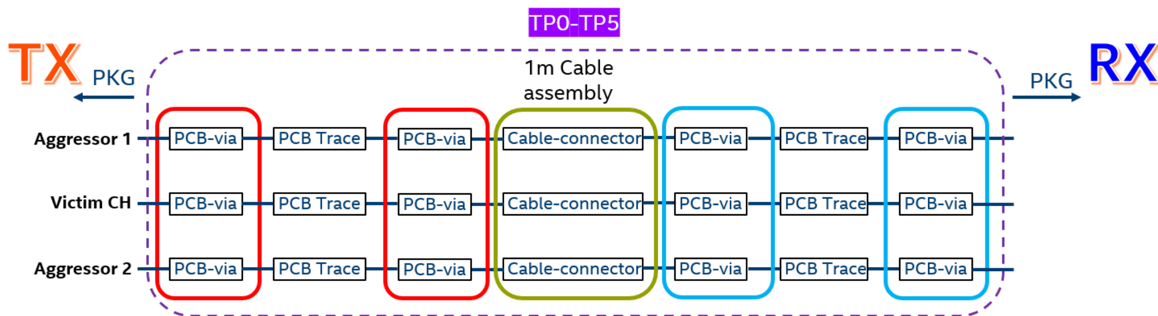

Fig. 3. Channel builder from TP0 to TP5 (ball-to-ball), 3-TX + 3-RX channels.

Figure 3 illustrates the channel model topology from TP0 to TP5, which consists of the optimized PCB via transitions for TX and RX, PCB trace models and cable/connector models. 3-pairs of TX and 3-pairs of RX are included for cross talk study. Cable and connector models are provided by Amphenol. Figure 4 shows the channel performance. It

is noticed that the TP0-TP5 insertion loss is -31.6dB, which is 1dB out of budget (refer to Figure 2), this is due to the cable loss of ~ 16.3dB vs. the budgeted 15dB. Differential return loss is better than -10dB, and cross talk better than -41.5dB up to 53GHz.

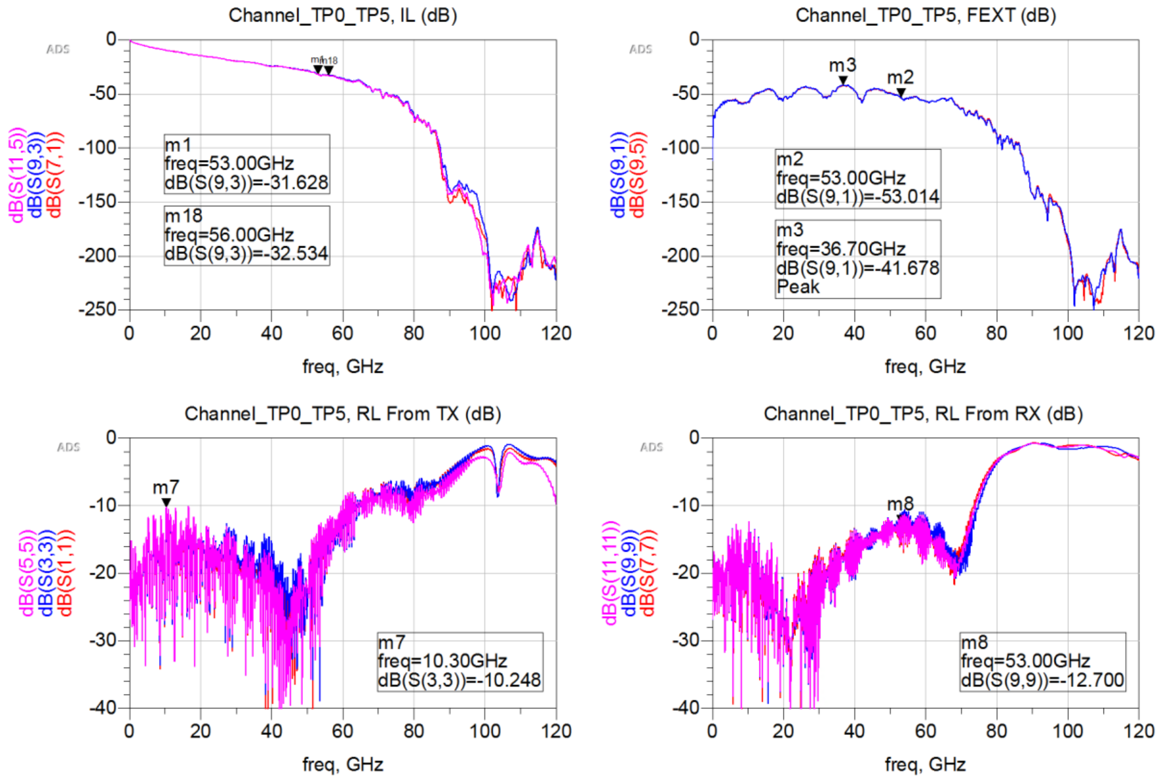

Fig. 4. Channel characteristics from TP0 to TP5 (Max PCB via length ~ 65mils, via stub length 4 mils, PCB trace TX+RX ~ 10-inch, 1-meter cable + 2 connectors), differential return loss better than -10dB, insertion loss ~ 31.6dB, FEXT ~ -41.5 dB, up to 53GHz.

A TDR is performed to check the discontinuities in the channel, and it is observed that the cable assembly contributes to the biggest discontinuities, as demonstrated in Figure 5.

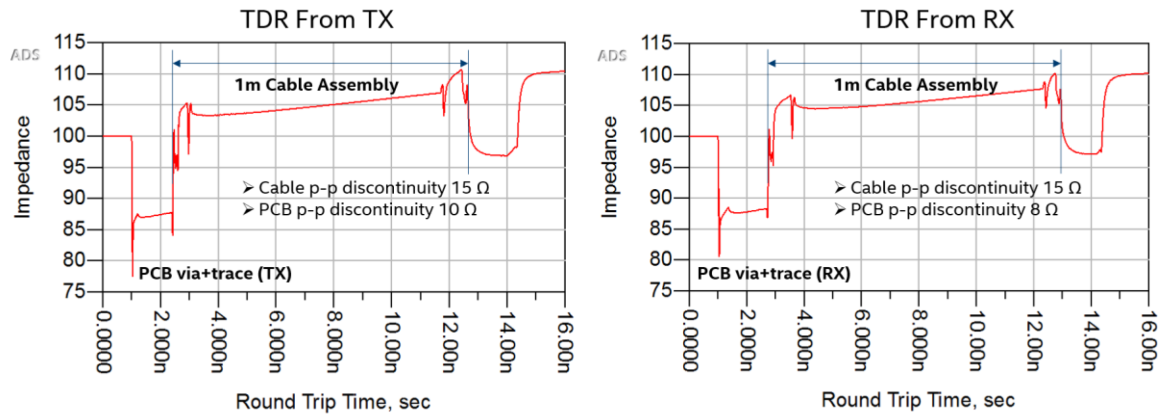

Fig. 5. TDR of channel TP0-TP5 (Tr=10ps). Cable peak-to-peak discontinuities are 15Ω, PCB peak-to-peak discontinuities are 8-10 Ω.

A well-engineered package design is used to connect with the above-described channel, as illustrated in Figure 6. By adjusting the package skip-layer trace length to compensate the extra 1dB cable assembly loss, the end-to-end channel characteristics are verified to meet the 40dB link budget. An accurate package-PCB interface modeling methodology is used to ensure the cascaded models are accurate in the frequency range of interest.

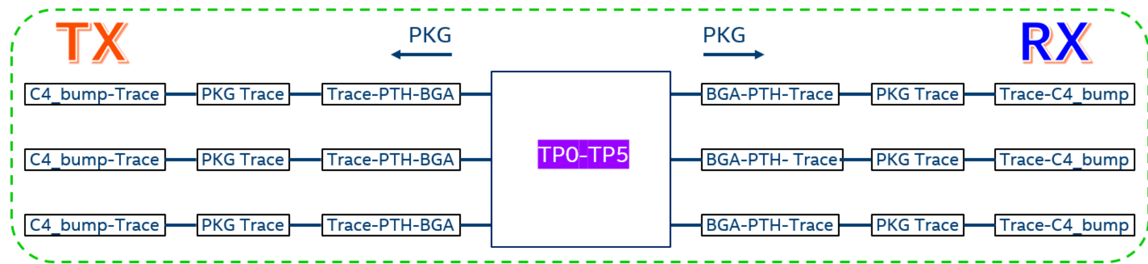

Fig. 6. End-to-end link builder, 3-TX + 3-RX (TX package + TP0-TP5 + RX package).

Figure 7 shows the end-to-end link performance of the optimized design. It can be seen that the 40dB link budget is verified with our proposed channel solutions.

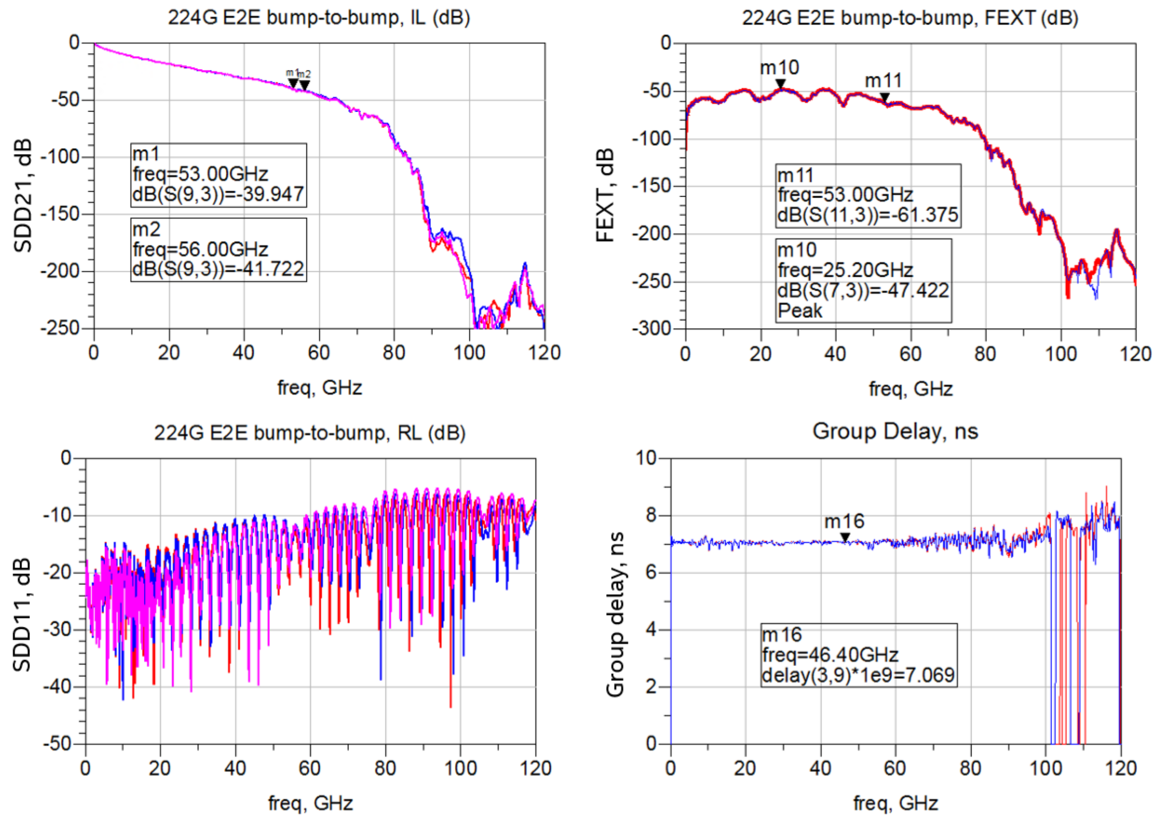

Fig. 7 End-to-End link performance of package, board, cable and connector (Package trace length 30mm one way, BGA ball pitch 0.8mm, 22 total package routing layers). Differential return loss better than -10dB, insertion loss ~ 40dB, FEXT ~ -47 dB, up to 53GHz.

The end-to-end channel solutions including the package and PCB design optimization, the package-PCB co-modeling methodology, the connector mating interface improvement, and the forward looking cable assembly features are described in the following chapters.

224Gbps-PAM4 Package Design

A 224Gbps-PAM4 package design practice was described in our 2021 DesignCon paper [1] where the higher-order mode propagation and dispersion, plane resonance, transmission loss, cross talk, multi-reflection, and package BGA ball pitch/ball pattern impact on the signal integrity was discovered. The vertical transition of a 0.5mm pitch BGA package was optimized to achieve the return loss of -15dB and cross talk of -100 dB to 56GHz, and the 1dB bandwidth to 68GHz.

The 0.5mm ball pitch, however, can only support small formfactor BGA packages. Large packages with high IO count require a larger ball pitch to minimize the package reliability risk. Based on the studies conducted in [1], up to 0.8mm ball pitch can be used to avoid the higher-order mode propagation. In this paper, a 0.8mm pitch BGA package was optimized to meet the similar performance goals of its 0.5mm counterpart. Figure 8 shows the differential return loss, insertion loss and differential TDR of the optimized 0.8mm package vertical transition (PTH-BGA ball).

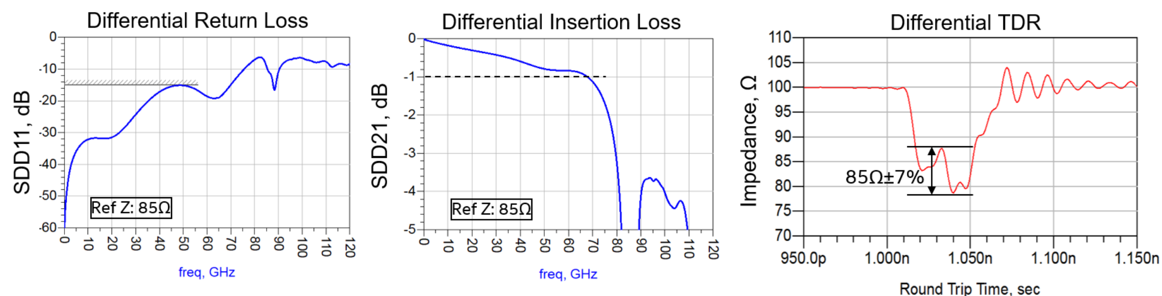

Fig. 8. Optimized package PTH-BGA transition with 0.8mm BGA ball pitch. Differential return loss better than -15dB, 1dB bandwidth to 68GHz, peak-to-peak discontinuities 85Ω±7%.

It can be seen that the package vertical loss drops significantly when the frequencies reach or exceed the cutoff frequency (~ 72GHz) of the 0.8mm ball pitch. In order to meet the package loss budget of 3.7dB with 30mm trace length, a skip-layer trace configuration is required in the global routing area [1][2] to attain an average trace loss of 0.123dB/mm at 53GHz, this can be realized with Intel next generation advanced substrate material.

224Gbps-PAM4 High-Density PCB Architectural Design

It has been observed that the channel performance deteriorates considerably when the operation frequencies go beyond 45GHz, and the already challenging electrical requirements of high bandwidth are further complicated by the consideration of high channel density. In this paper, a novel PCB architectural design is introduced to deal with up to 512 lanes operating at 224Gbps-PAM4 data rate per lane.

BGA ball patterning directly impacts the PCB via cross talk, and the via loss, and should be carefully engineered to meet the PCB vertical loss target, as well as the cross talk requirement. A well designed ball pattern also benefits the PCB trace breakout. In this paper, a 0.8mm pitch ball pattern is first identified in the package-PCB co-design. The outer BGA rows are allocated to TX and inner rows to RX. Differential ball pairs are fully shielded with ground balls. Two rows of ground shielding are utilized between TX and RX to mitigate the TX to RX near-end cross talk, as illustrated in Figure 9.

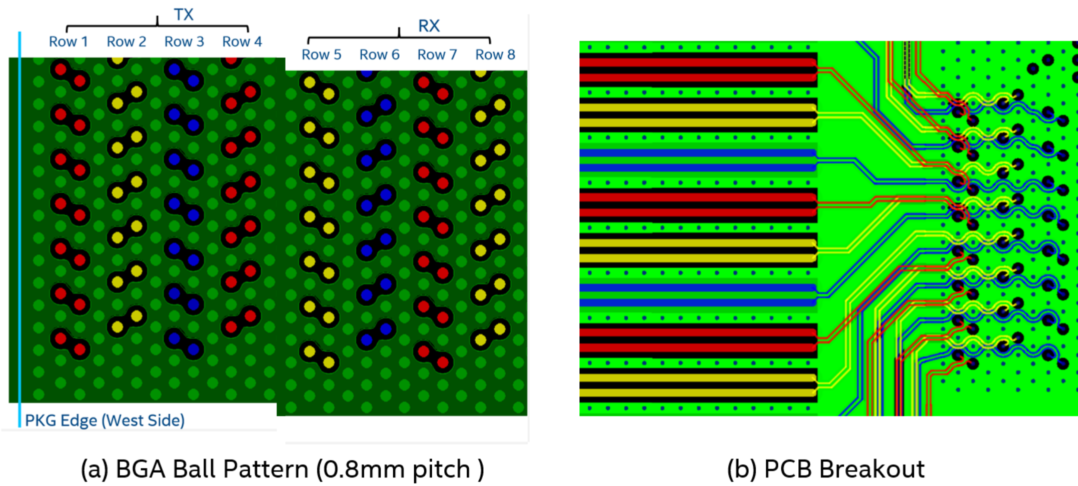

Fig. 9. BGA ball pattern and PCB breakout. Outer rows for TX, inner rows for RX, two rows of ground shielding between TX and RX. Different rows breakout to different routing layers.

In order to minimize the PCB vertical loss and cross talk, shallow PCB layers are recommended for SerDes signal routing, and a skip-layer trace configuration is required that can significantly reduce the trace loss. A 0.95 dB/inch loss can be achieved with 85Ω differential skip-layer configuration in the global routing area, as shown in Figure 10.

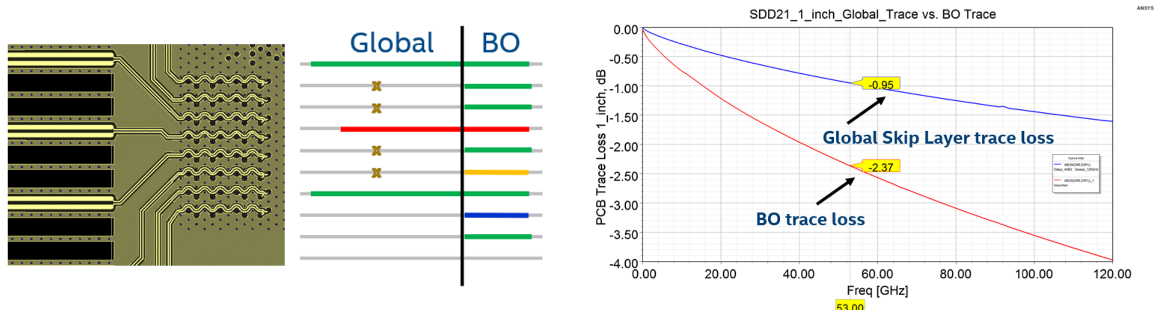

Fig. 10. PCB trace configuration, global area skip-layer vs. breakout (BO) area trace loss.

Figure 11 shows a recommended PCB stackup and channel distribution for a 512-channel board design. All TX and RX traces are routed using top PCB layers. This requires a PCB technology improvement to address the copper balance and the planarity concern. One of the mitigation ways is to use a thick core. 8 signal routing layers are required to accommodate the 512 channels with 64 channels per layer, as shown in Figure 11.

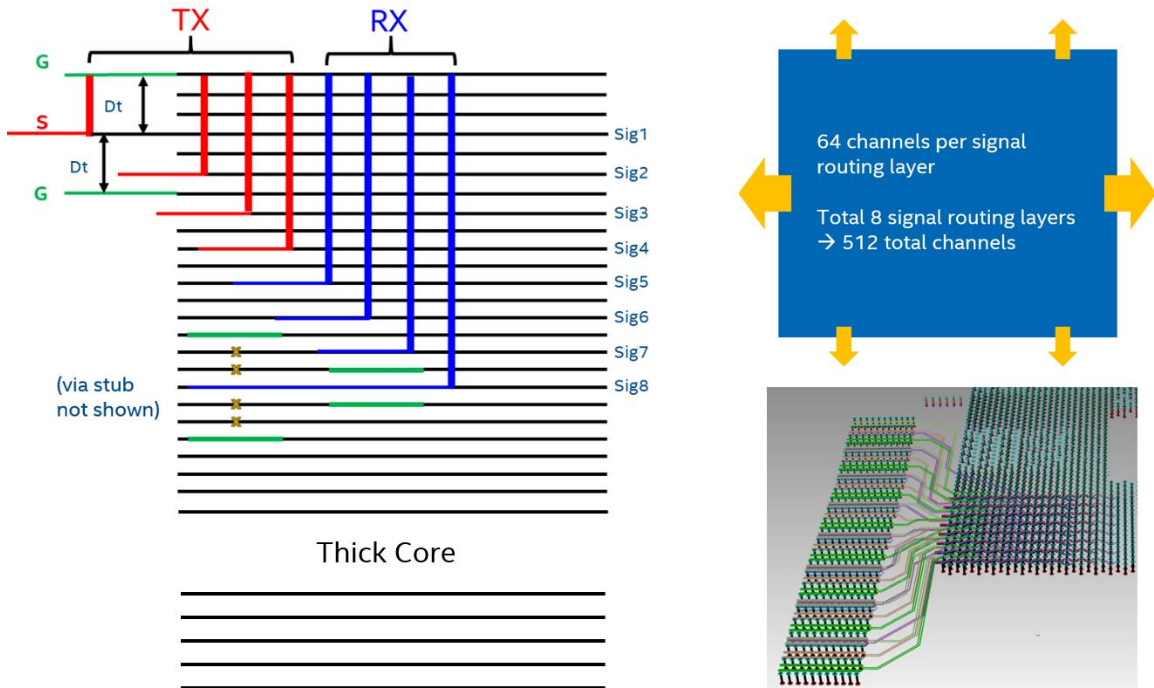

Fig. 11. Recommended PCB stackup and channel distribution for a 512-channel board design.

Due to the implementation of the skip-layer trace routing, the deepest signal routing layers for TX and RX are Layer 10 and Layer 18. The optimization of the PCB vertical transitions was performed for L10 and L18 via where the via length is ~ 35mils and 65mils respectively in this case study. Figure 12 shows the optimization results of the L18 via transition.

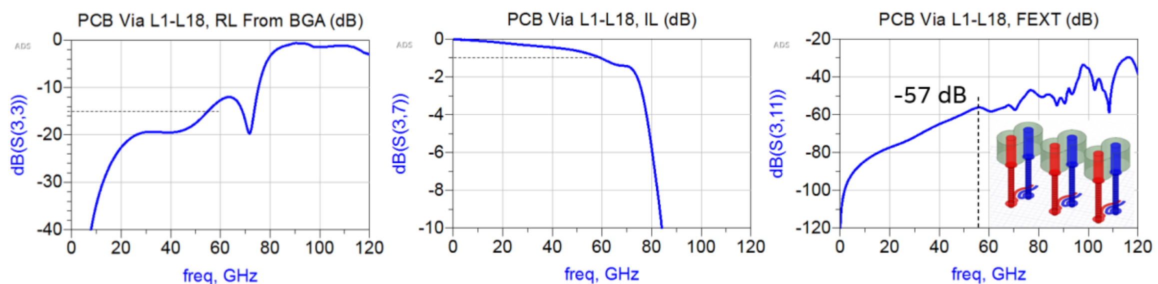

Fig. 12. PCB via transition L1-L18, ~ 65 mil via length with 4 mil via stub. 1dB bandwidth to 59GHz, return loss better than -15dB to 55GHz, far-end cross talk better than -57 dB to 53GHz.

Accurate Package-PCB Co-Modeling

The package and PCB are often designed separately, and the optimized package and PCB models are then cascaded for performing a link simulation. The BGA ball is included in the package model and should not be double counted in the PCB model. How to terminate the PCB ball pad and accurately model the package-PCB interface becomes critical in the PCB modeling. In this paper, a coax port at the package-PCB interface is designed that accurately captures the pad capacitance yet not introduces extra discontinuities. The coax port uses an inner conductor that carries the BGA ball diameter, and an outer conductor following the BGA shielding pattern. The insulating material is optimized to demonstrate an 85Ω differential impedance to mitigate the port discontinuities. Figure 13 shows the correlation results of the cascaded package and PCB models vs. the united package-PCB model. Good correlations of TDR and differential return loss, insertion loss, propagation phase to 80GHz can be obtained using this methodology. The optimized port configuration was used in the PCB modeling for the link budget analysis.

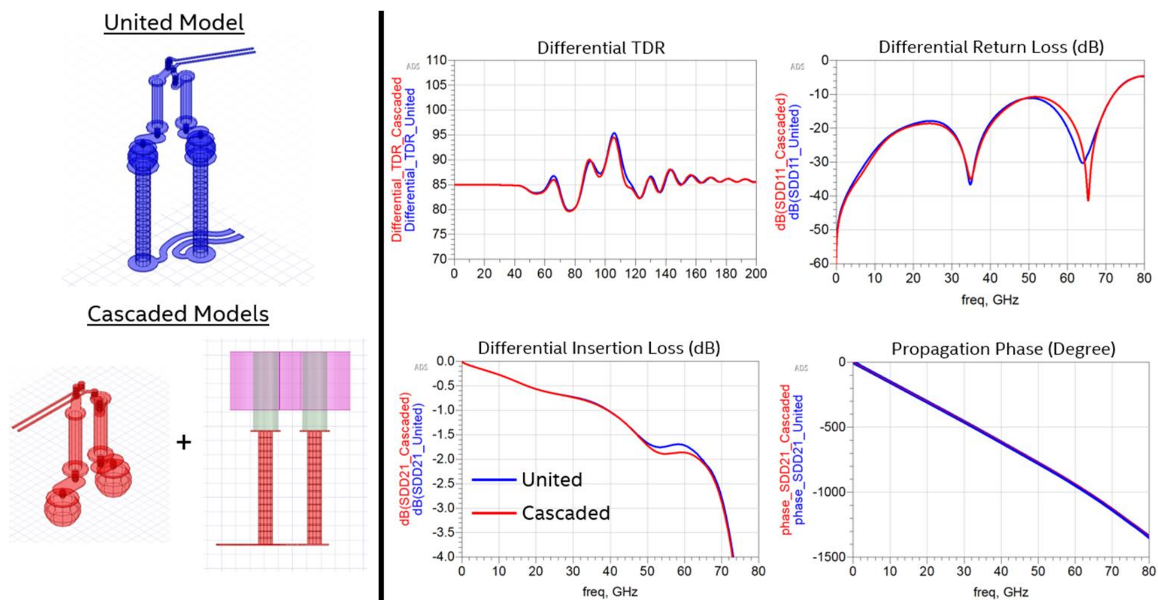

Fig. 13. Correlation of cascaded package+PCB models vs. united packge-PCB model. Good correlation of TDR and differential return loss, insertion loss, propagation phase to 80GHz.

Cable-Connector Requirement and Forward Looking

In the 224Gbps link system discussed in this paper, the cable/connector takes about 40% of the link budget and becomes the gating factor in enabling the PAM4 modulation in a high-density long-reach networking system. A desired next generation cable assembly (1-

meter cable + 2 connectors) loss target for interpretation flexibility is 10dB to 53GHz. The general cable/connector design practice is not within the scope of this study. In this paper, we explored the design improvement of the SMT connector interface and used an OSFP connector as an example to study the connector interface. It is observed that by reducing the connector pad stub length from current 27mils to 10mils, the loss can be reduced by 1.6dB, as shown in Figure 14. In a 2-connector system, the loss improvement is 3.2dB, this allows ~ 3-inch longer PCB trace routing.

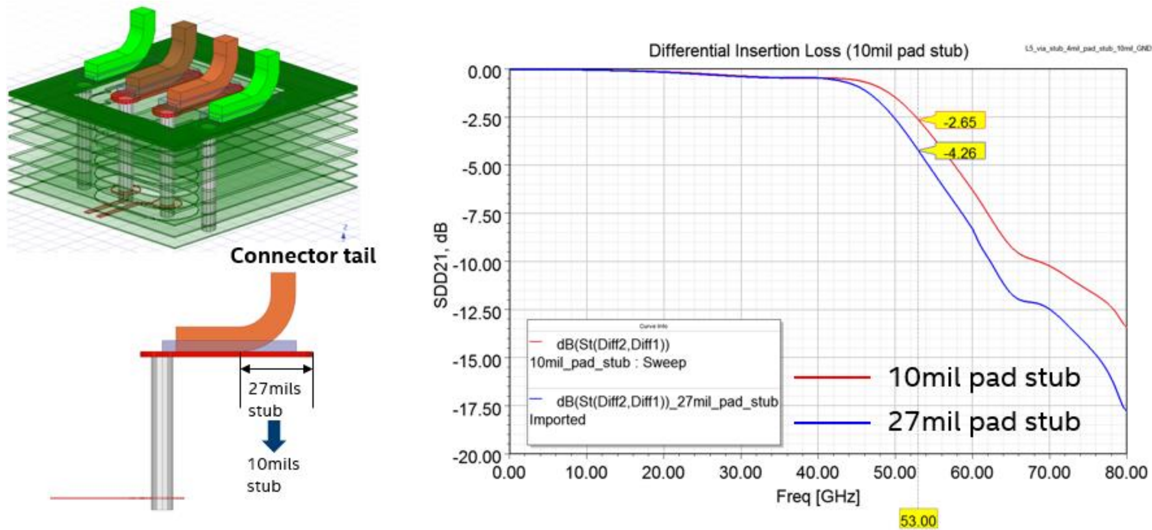

Fig. 14. Design improvement of SMT connector interface. 1.6dB loss improvement can be achieved by reducing the stub length of the landing pad from current 27mils to 10mils.

Summary

In this paper, a 40dB end-to-end link budget was proposed for a high-density 100T networking/switching system operating at 224Gbps-PAM4 data rate per lane (53GHz Nyquist frequency). The system includes a bi-directional IEEE 802.3 reference package of 30mm (one way) trace length, a high-density board of up to 512 lanes with 10-inch TX+RX PCB routing length, a 1-meter cable and two connectors. The loss breakdown was analyzed for the package, board, cable, and connector.

Skip-layer trace design is the key enablement to the trace loss reduction, and a careful PCB architectural design is essential to meet the vertical loss and cross talk requirements of a high-density board. In the package design, the 1dB vertical loss target can be achieved with 0.8mm ball pitch, ≤ 1mm core thickness, and up to 22 package layer count; the 0.123 dB/mm average trace loss requires a skip-layer trace design in the global routing area and advanced substrate material. In the PCB design, shallow layers are recommended for SerDes trace routing. The via length of the signal routing layer should be less than 65 mils and via stub length smaller than 6 mils; the 0.95 dB/inch PCB trace loss in the global routing area requires a skip-layer trace configuration and low loss PCB

material. The projected cable assembly loss is 15dB if considering the backward compatibility requirement. The desired next generation cable assembly loss is 10dB with the new technology to enable the increase of the cutoff frequency. The design optimization of a connector mating interface was also discussed in this paper and a 3.2dB loss improvement is observed for the 2-connector cable assembly.

An accurate package-PCB co-modeling methodology was proposed that uses a carefully engineered coax port to terminate the BGA ball pad on the PCB. A good correlation of the cascaded package and PCB models vs. the united package-PCB model can be attained from DC to 80GHz.

The exploratory approaches described in this paper drive the key enablement solutions to a successful 224Gbps-PAM4 high-density 100T networking/switching system design.

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